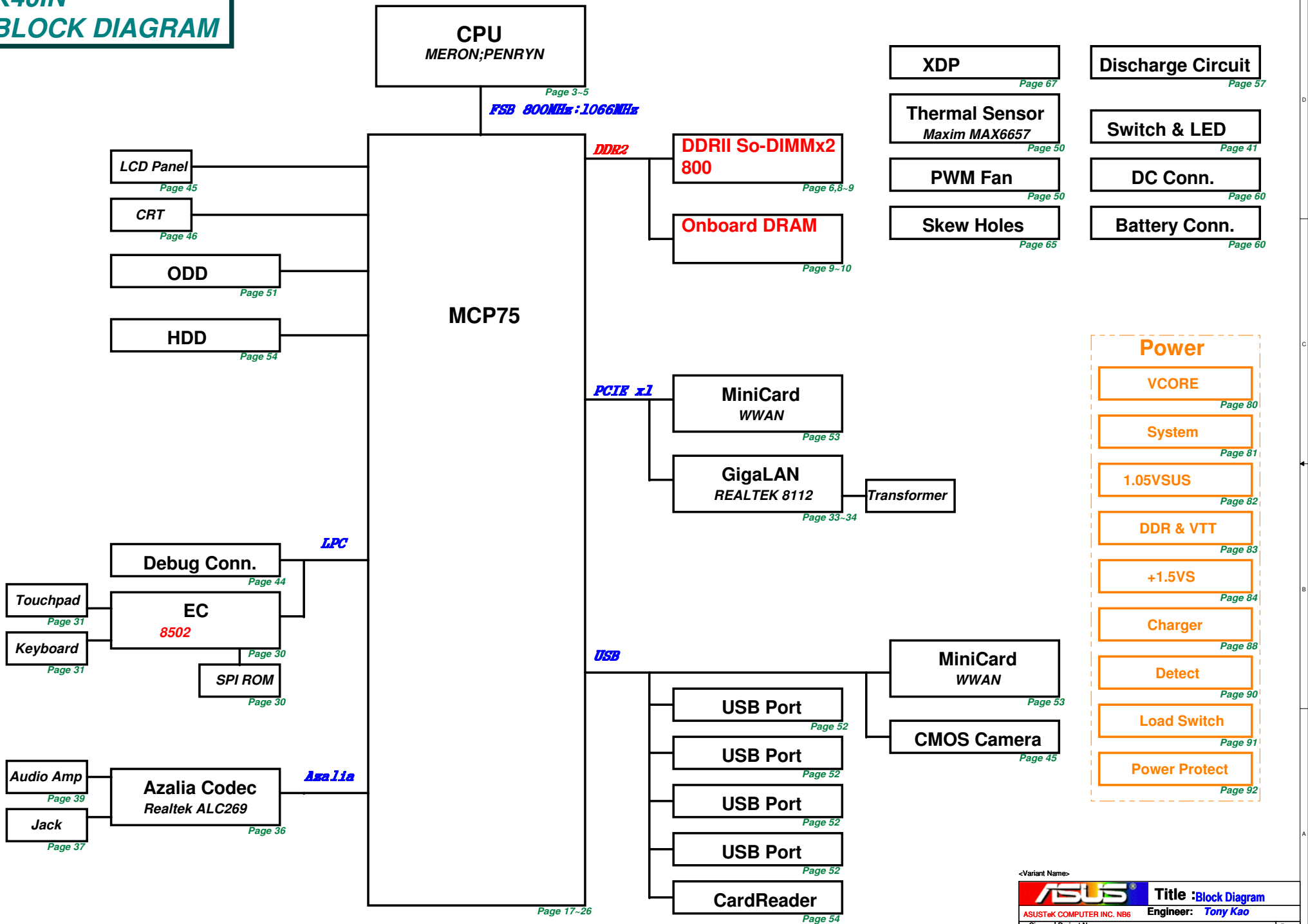
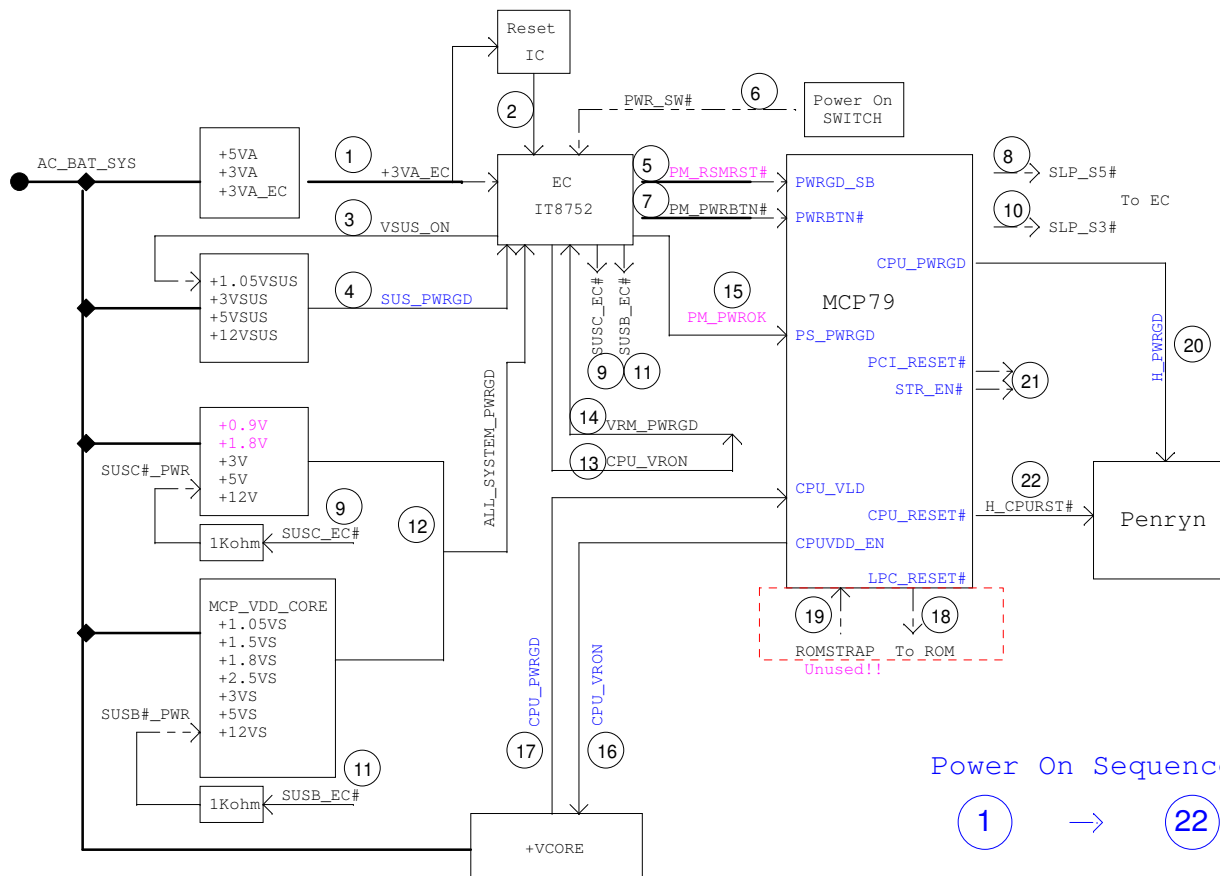


K40IN BLOCK DIAGRAM



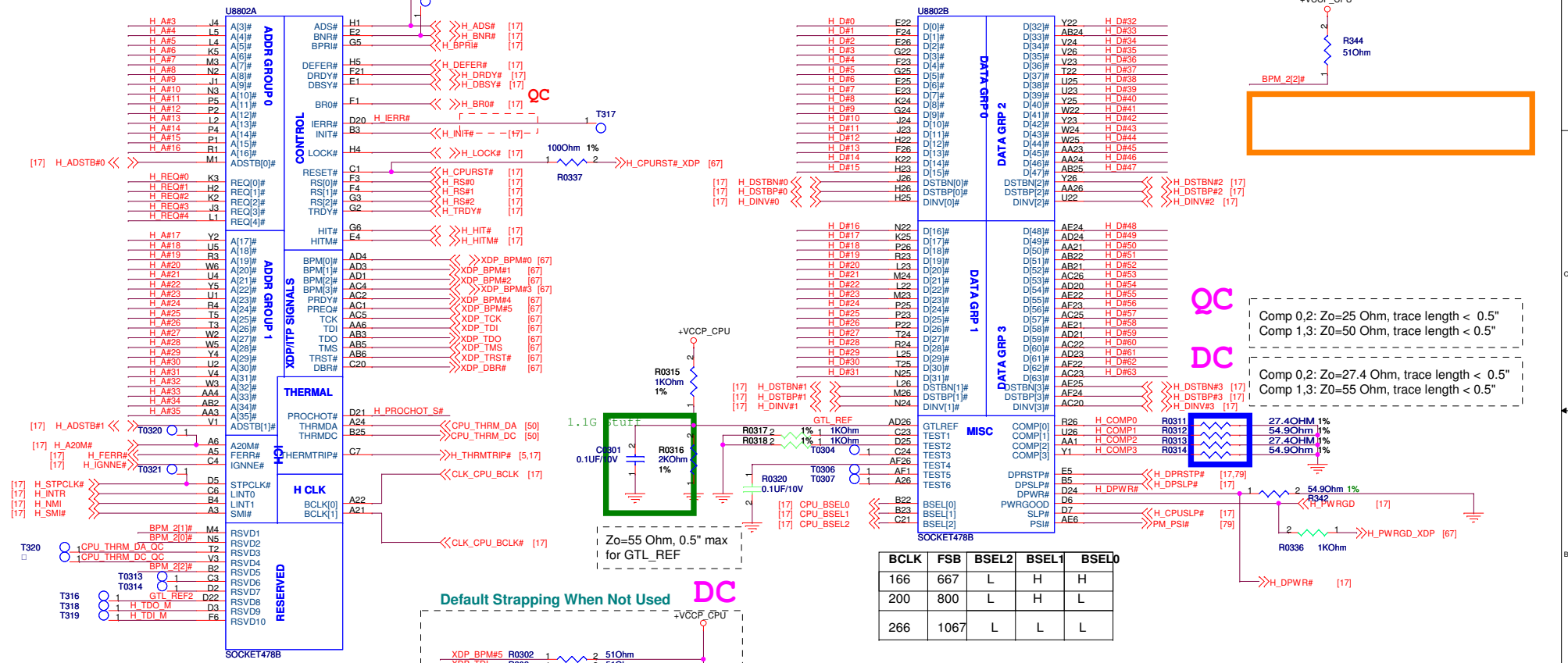


Power On Sequence



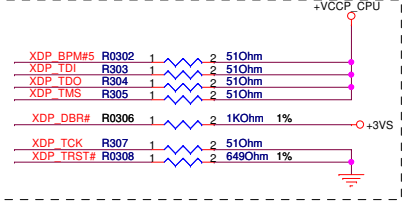
[17] H_D#[63:0] << H_D#[63:0]
 [17] H_A#[35:3] << H_A#[35:3]
 [17] H_REQ#[4:0] << H_REQ#[4:0]

Place beside CPU ball out



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

Default Strapping When Not Used DC



Place R304 & R306 for XDP function

Default Strapping When Not Used QC

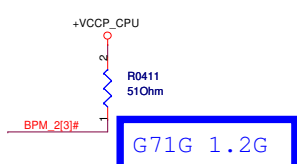
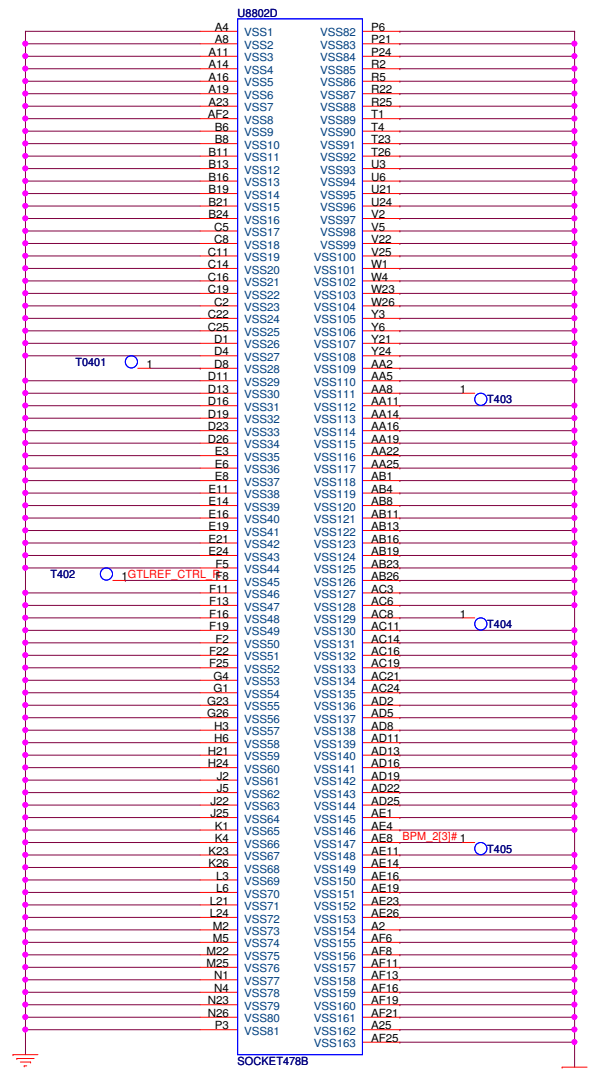
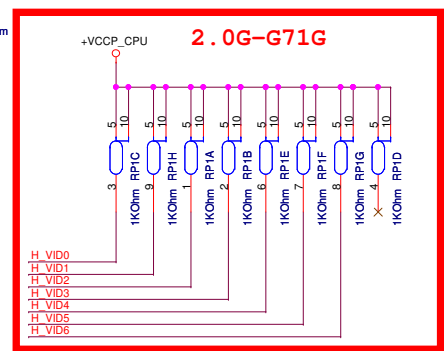
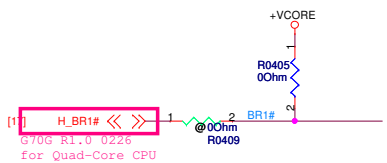
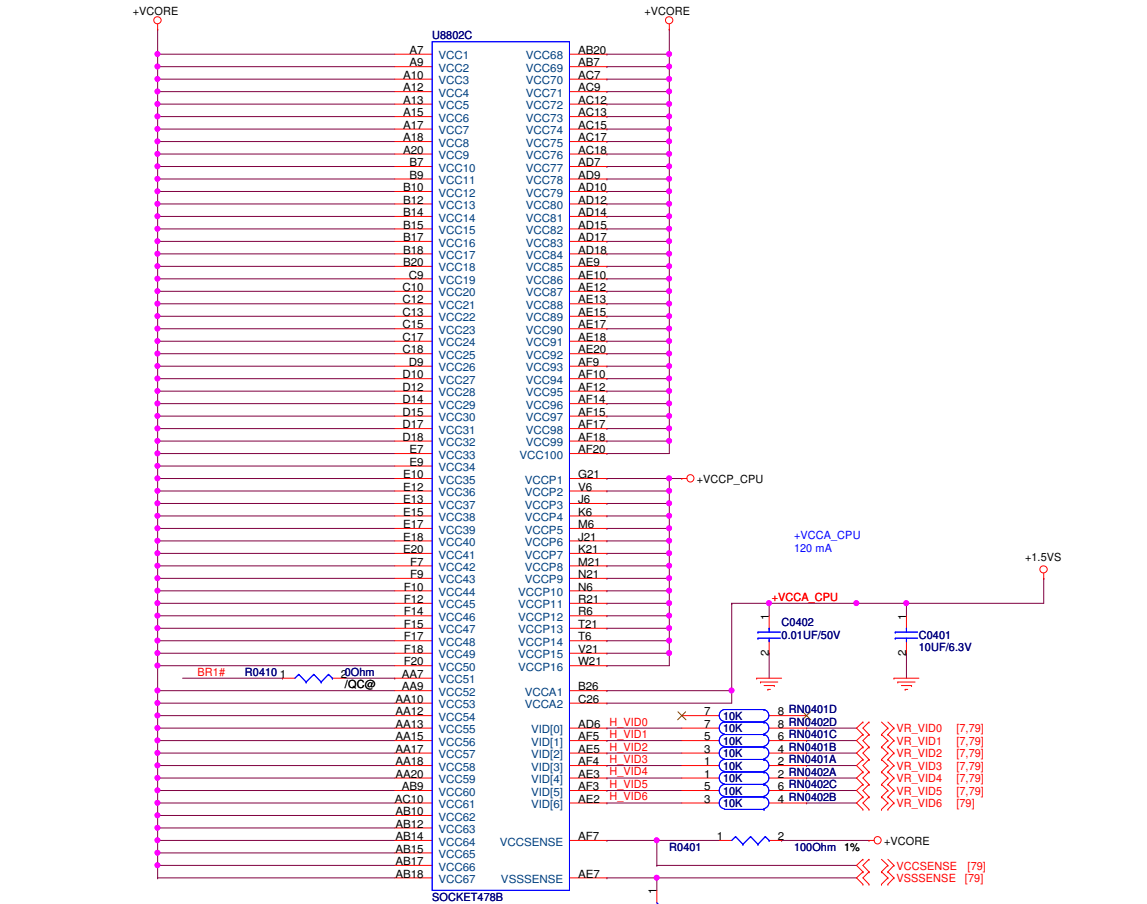


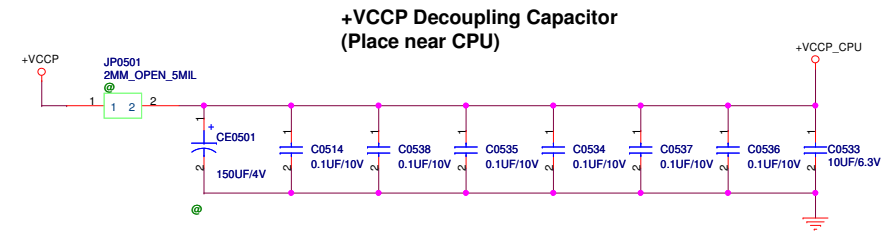
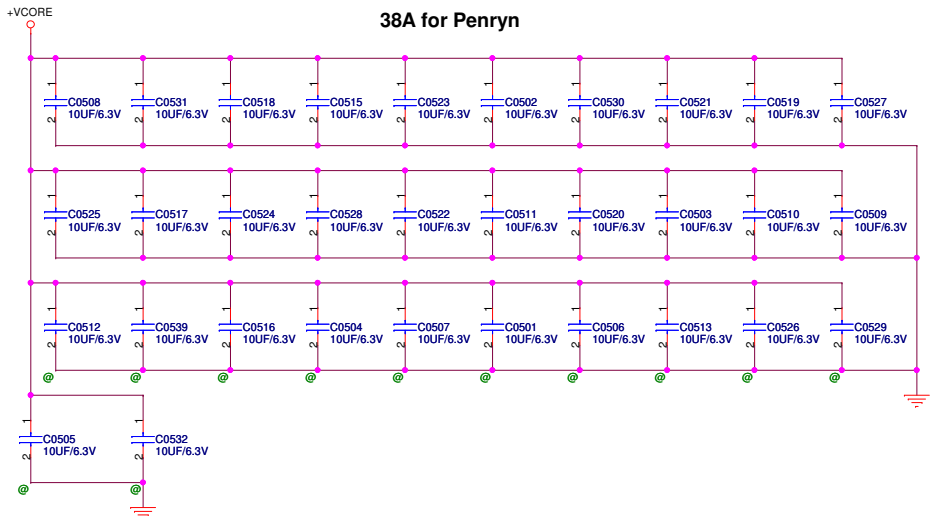
Comp 0,2: Zo=25 Ohm, trace length < 0.5"
 Comp 1,3: Zo=50 Ohm, trace length < 0.5"
 Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
 Comp 1,3: Zo=55 Ohm, trace length < 0.5"

ASUS Title : Penryn CPU (1)
 Engineer:
 Size Project Name Rev 1.0
 Custom Date: Friday, February 13, 2009 Sheet 3 of 91

Pin B2 M4 N5 left as NC for QC Pin T2 V3 change to design (BPM_2# [2] BPM_2#[1]) QC Thermal Diode detect (THRMDA_2 BPM_2[0])

mount QC : /QC
 unmount QC : /QC@



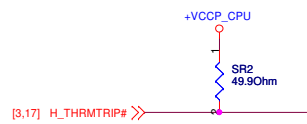


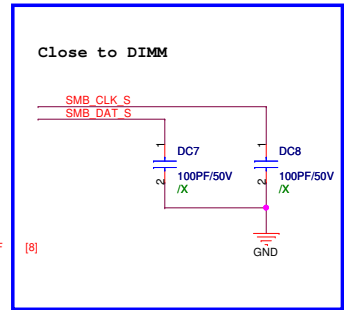
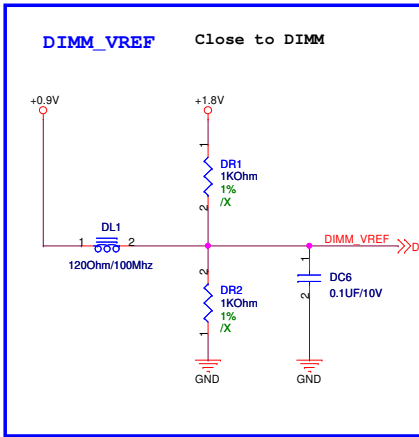
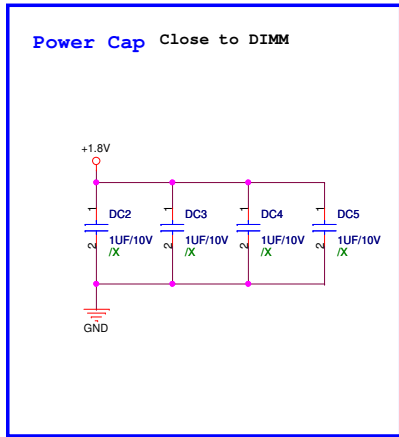
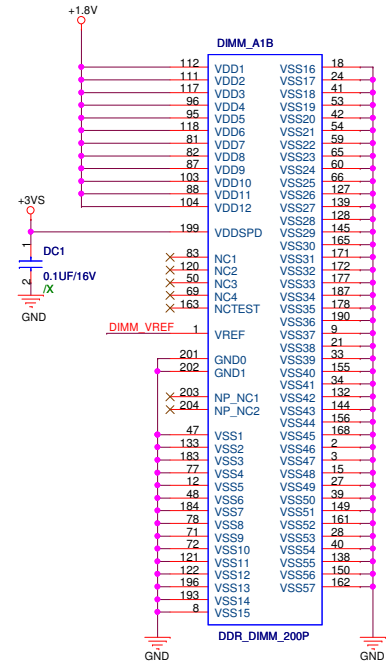
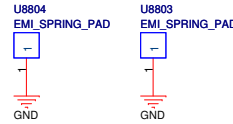
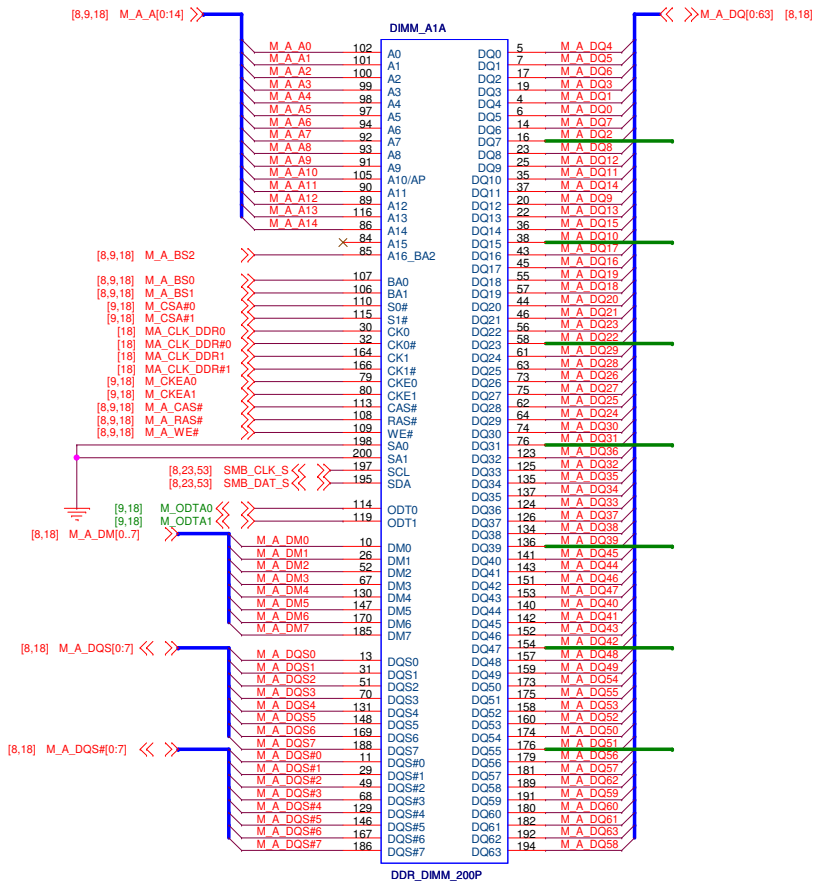
Decoupling guide from Intel

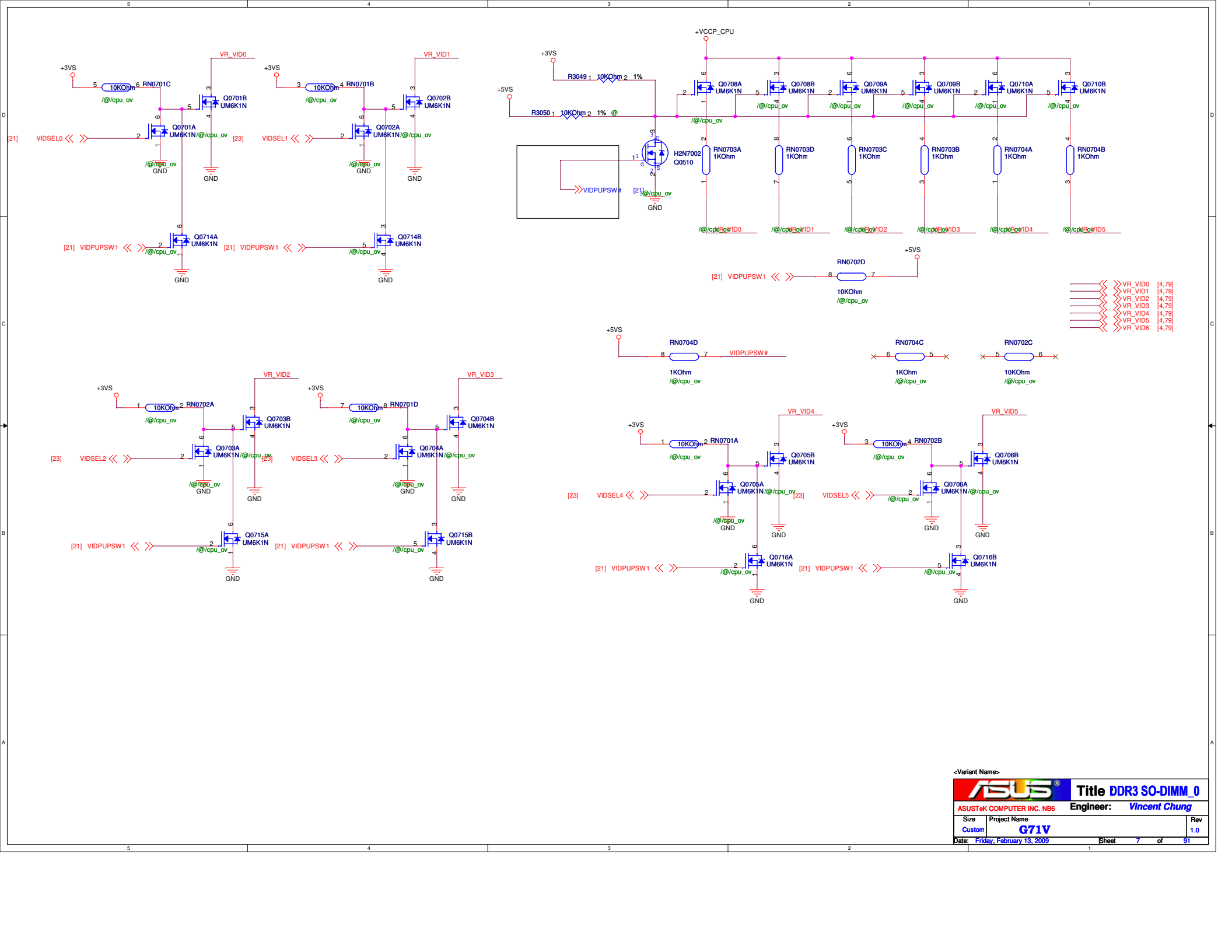
V CORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

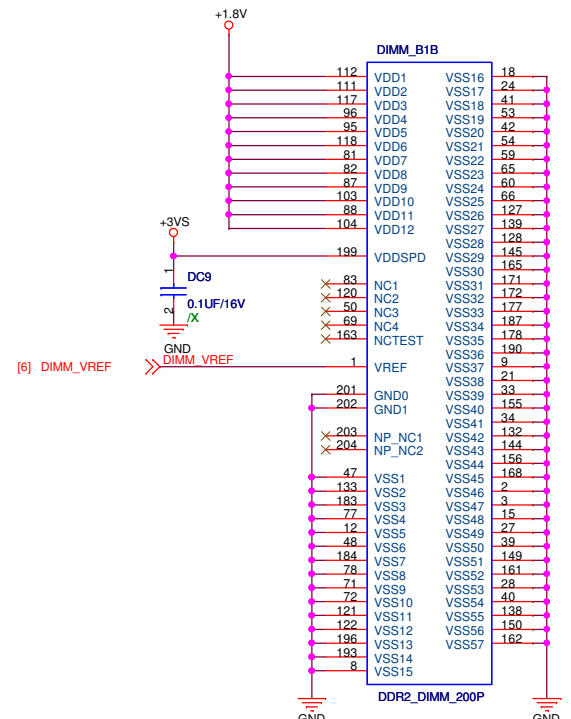
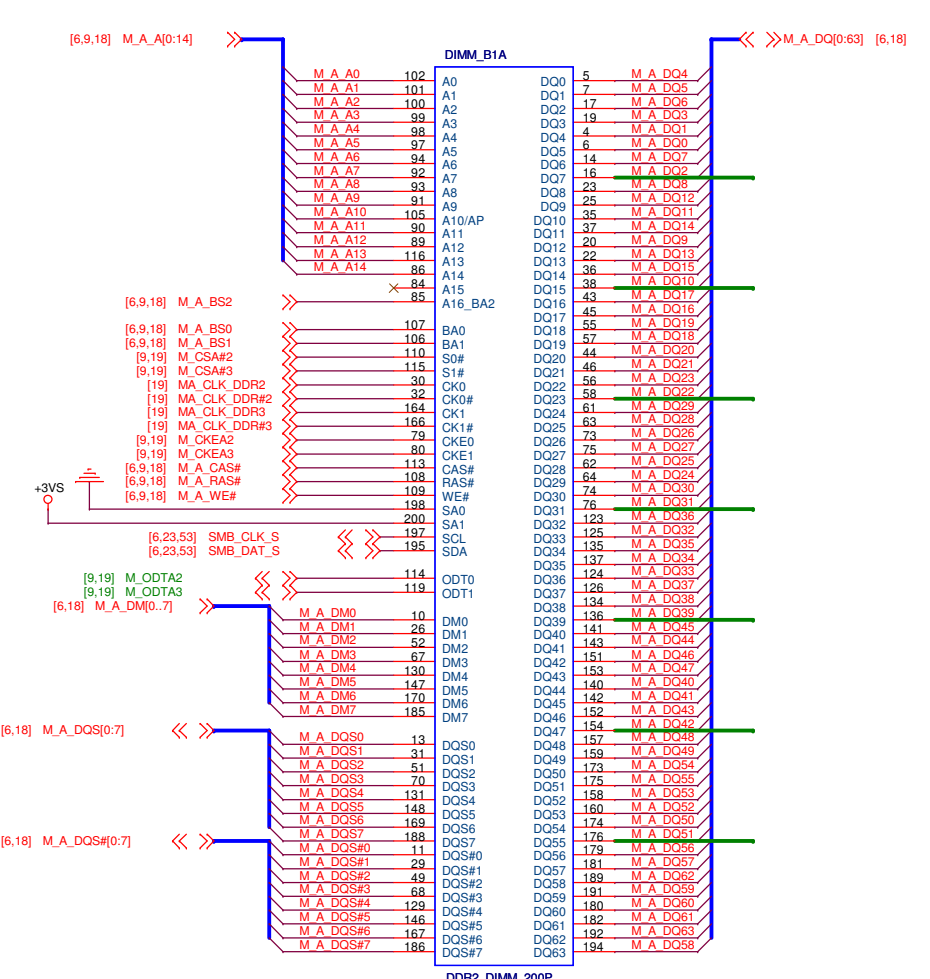
+V CORE Mid-Frequency Capacitor
 Intel: 22UF *32
 F3S: 10UF *16
 A7S: 10UF *1011/17
 V1V: ?

+VCCP Decoupling Capacitor
 Intel: 270UF *1, 0.1UF *6
 F3S: 100UF *1, 0.1UF *4
 V1V: ?









1.1G modify P/N

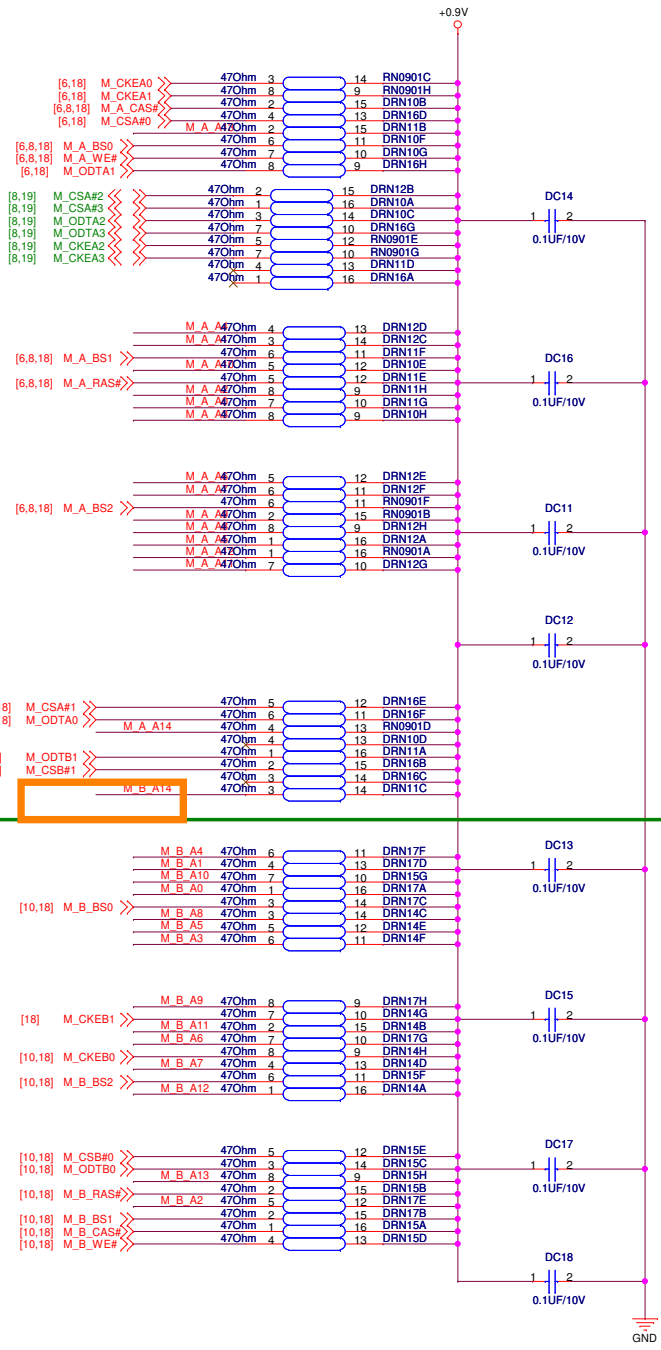
1.1G modify P/N

<Variant Name>

ASUS		Title DDR3 SO-DIMM_1	
ASUSTek COMPUTER INC. NB6		Engineer: Vincent Chung	
Size B	Project Name G71V	Sheet 8	of 91
Date: Friday, February 13, 2009			

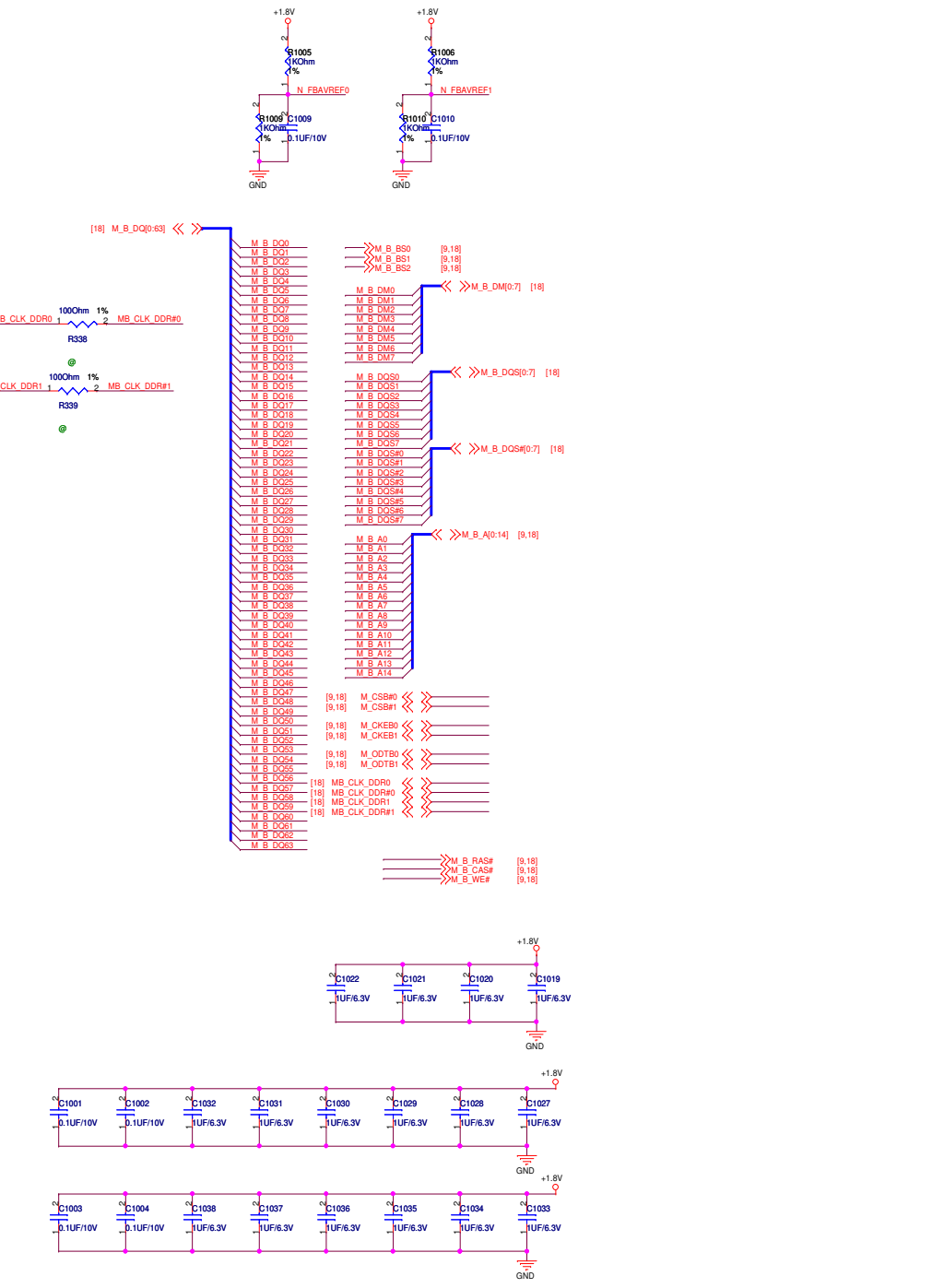
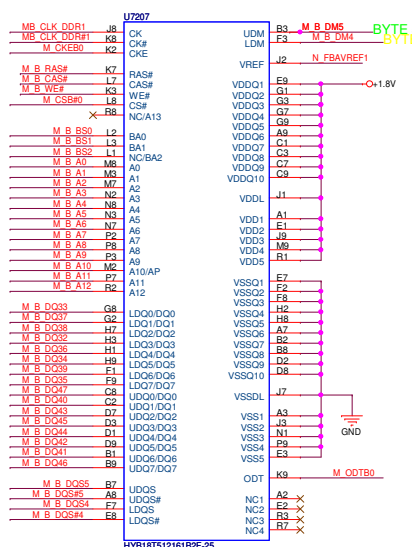
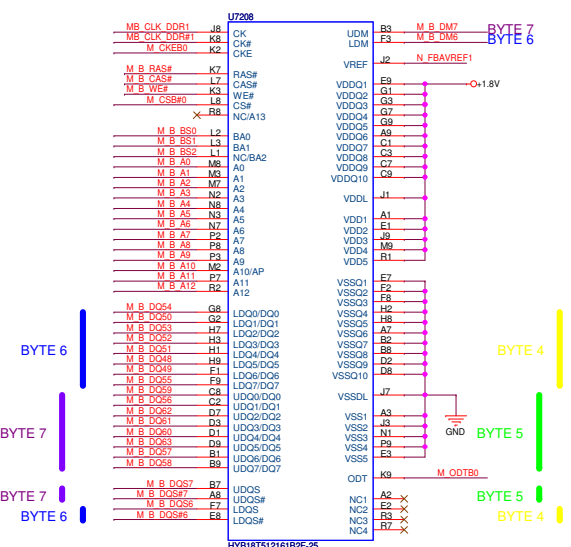
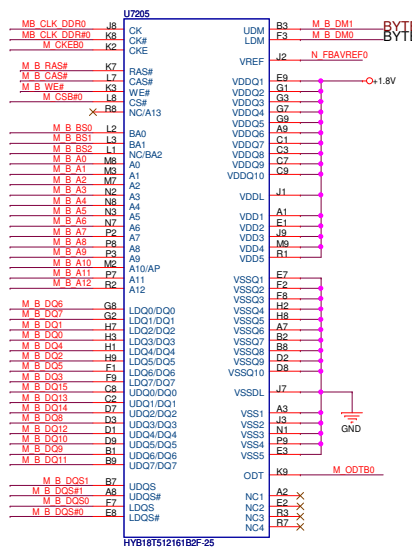
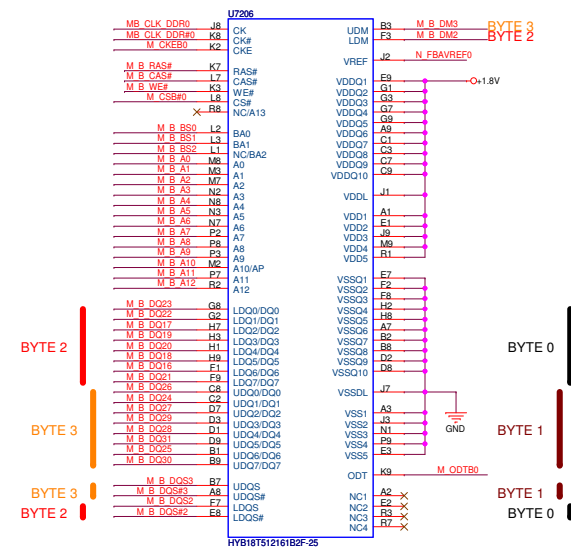
<< >>M_A_A[0:14] [6,8,18]

<< >>M_B_A[0:14] [10,18]




<Variant Name>

		Title DDR3 termination	
ASUSTek COMPUTER INC. NBS		Engineer: Vincent Chung	
Size	Project Name	Size	Rev
Custom	G71V		1.0
Date: Monday, February 16, 2009		Sheet	9 of 91




<Variant Name>

		Title : Cantiga-DDR3/PEG(2)
Engineer:		
Size	Project Name	Rev
C		1.0
Date: <u>Friday, February 13, 2009</u>		Sheet: <u>11</u> of <u>91</u>




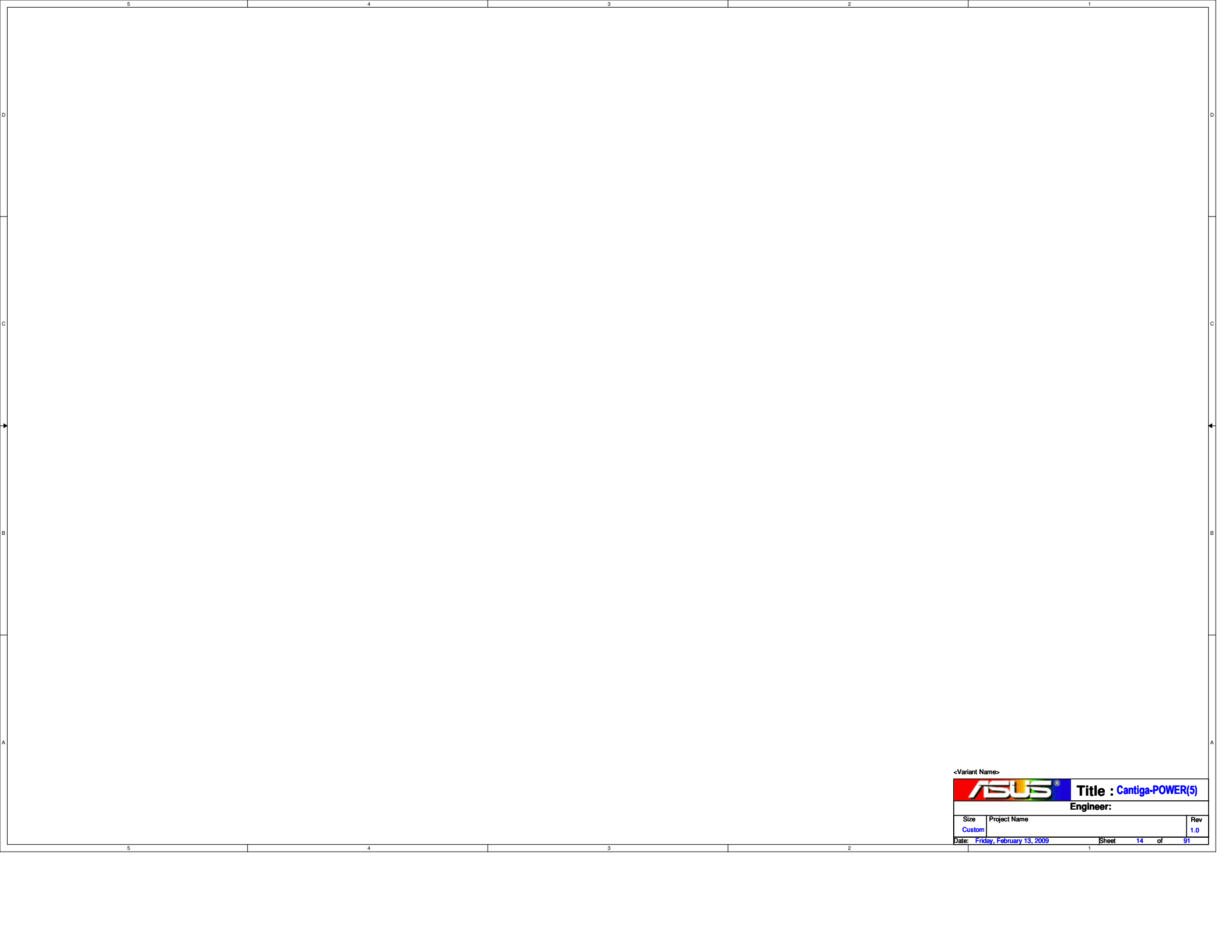
<Variant Name>

		Title : Cantiga-DDR3 bus (3)
Engineer:		
Size	Project Name	Rev
C		1.0
Date: Friday, February 13, 2009		Sheet 12 of 91




<Variant Name>

		Title : Cantiga-POWER (4)
Engineer:		
Size	Project Name	Rev
C		1.0
Date: Friday, February 13, 2009		Sheet 13 of 91



-Variant Name-

		Title : Cantiga-POWER(5)
Engineer:		
Size	Project Name	Rev
Custom		1.0
Date: Friday, February 13, 2009		Sheet 14 of 91

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : Cantiga-GND	
Engineer:			
Size	Project Name		Rev
B			1.0
Date: Friday, February 13, 2009		Sheet	15 of 91

5

4

3

2

1

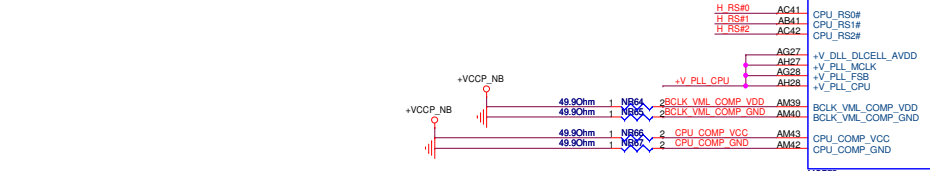
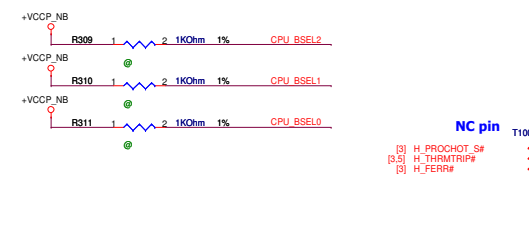
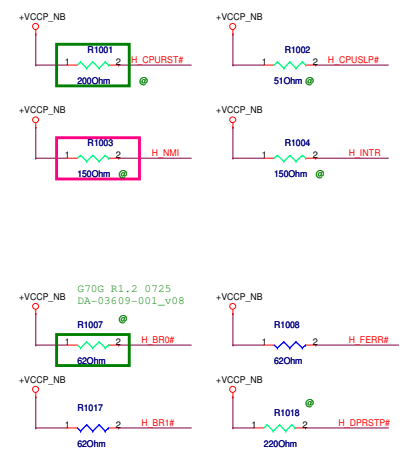
NU1A

H_DSTBP#0	T40	CPU_DSTBP0#
H_DSTBN#0	U40	CPU_DSTBN0#
H_DIN#0	V41	CPU_DBI0#
H_DSTBP#1	W39	CPU_DSTBP1#
H_DSTBN#1	W37	CPU_DSTBN1#
H_DIN#1	Y35	CPU_DBI1#
H_DSTBP#2	N37	CPU_DSTBP2#
H_DSTBN#2	L38	CPU_DSTBN2#
H_DIN#2	N35	CPU_DBI2#
H_DSTBP#3	M39	CPU_DSTBP3#
H_DSTBN#3	M41	CPU_DSTBN3#
H_DIN#3	J41	CPU_DBI3#
H_A#3	AC34	CPU_A3#
H_A#4	AE36	CPU_A4#
H_A#5	AE34	CPU_A5#
H_A#6	AC37	CPU_A6#
H_A#7	AE37	CPU_A7#
H_A#8	AE35	CPU_A8#
H_A#9	AB35	CPU_A9#
H_A#10	AE35	CPU_A9#
H_A#11	AG35	CPU_A10#
H_A#12	AG39	CPU_A12#
H_A#13	AE33	CPU_A13#
H_A#14	AG37	CPU_A14#
H_A#15	AG38	CPU_A15#
H_A#16	AG34	CPU_A16#
H_A#17	AN38	CPU_A17#
H_A#18	AL39	CPU_A18#
H_A#19	AG33	CPU_A19#
H_A#20	AL33	CPU_A20#
H_A#21	AE31	CPU_A21#
H_A#22	AN36	CPU_A22#
H_A#23	AJ35	CPU_A23#
H_A#24	AJ35	CPU_A23#
H_A#25	AJ36	CPU_A24#
H_A#26	AJ38	CPU_A25#
H_A#27	AL37	CPU_A26#
H_A#28	AL34	CPU_A27#
H_A#29	AN37	CPU_A28#
H_A#30	AJ37	CPU_A29#
H_A#31	AL38	CPU_A30#
H_A#32	AN34	CPU_A31#
H_A#33	AL35	CPU_A32#
H_A#34	AN34	CPU_A33#
H_A#35	AR39	CPU_A34#
H_A#35	AN35	CPU_A35#
H_ADSTB#0	AE38	CPU_ADSTB0#
H_ADSTB#1	AK35	CPU_ADSTB1#
H_REQ#0	AC38	CPU_REQ0#
H_REQ#1	AK33	CPU_REQ1#
H_REQ#2	AC39	CPU_REQ2#
H_REQ#3	AC33	CPU_REQ3#
H_REQ#4	AC35	CPU_REQ4#

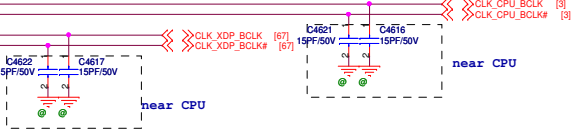
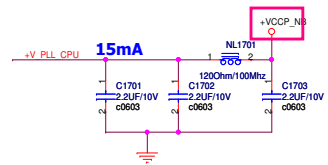
SEC 1 OF 11

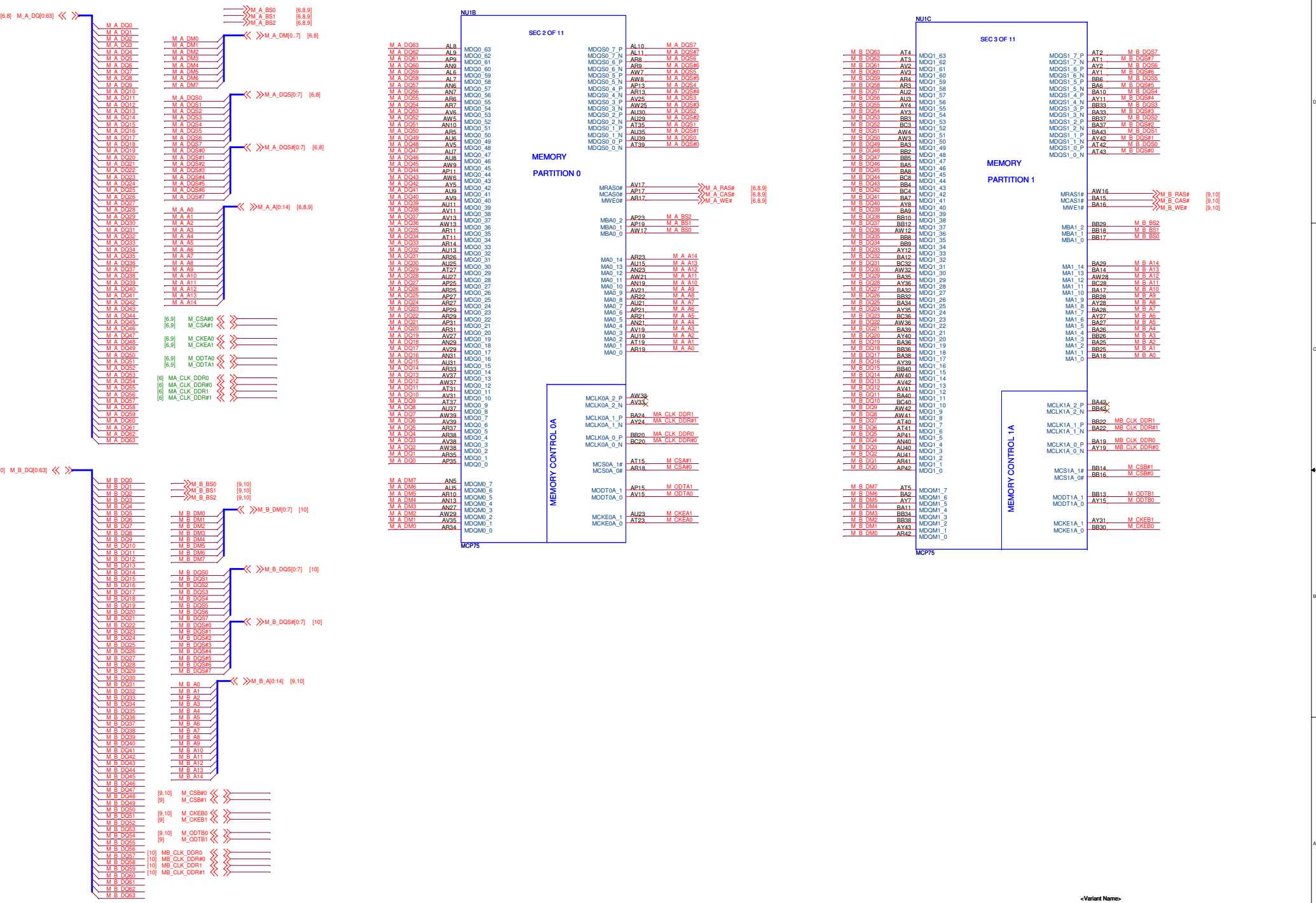
FSB

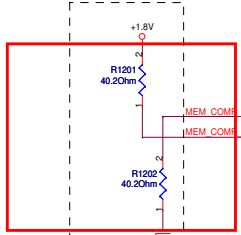
Y43	H_D#0
W42	H_D#1
Y40	H_D#2
W41	H_D#3
Y39	H_D#4
W42	H_D#5
Y41	H_D#6
Y42	H_D#7
L41	H_D#8
E42	H_D#9
L42	H_D#10
T41	H_D#11
E41	H_D#12
L43	H_D#13
W35	H_D#14
W37	H_D#15
W33	H_D#16
W34	H_D#17
AA35	H_D#18
AA34	H_D#19
AA38	H_D#20
AA35	H_D#21
U38	H_D#22
L36	H_D#23
L35	H_D#24
U33	H_D#25
U34	H_D#26
W38	H_D#27
E33	H_D#28
U34	H_D#29
W34	H_D#30
L37	H_D#31
N34	H_D#32
N33	H_D#33
D34	H_D#34
P35	H_D#35
P35	H_D#35
R38	H_D#36
R37	H_D#37
R38	H_D#38
L37	H_D#39
L37	H_D#40
L39	H_D#41
L38	H_D#42
N36	H_D#43
N38	H_D#44
N39	H_D#45
N38	H_D#46
L39	H_D#47
L37	H_D#48
L42	H_D#49
L42	H_D#49
P41	H_D#50
N41	H_D#51
N40	H_D#52
M40	H_D#53
H40	H_D#54
K42	H_D#55
H41	H_D#56
H41	H_D#57
L41	H_D#58
H42	H_D#59
K41	H_D#60
U40	H_D#61
L39	H_D#62
M45	H_D#63
AA41	H_BPR# [3]
AA40	H_DEFER# [3]
G42	CLK_CPU_BCLK [3]
G41	CLK_CPU_BCLK# [3]
AL43	CLK_XDP_BCLK [67]
AL42	CLK_XDP_BCLK# [67]
BCLK_OUT_ITP_P	AL41 BCLK FEEDBACK P
BCLK_OUT_ITP_N	AK42 BCLK FEEDBACK N
BCLK_OUT_NB_P	AK41
BCLK_OUT_NB_N	AK40
CPU_A30M#	AE41
CPU_IGNNE#	AH39
CPU_INTR	AH42
CPU_INTR#	AG41
CPU_SMI#	AH41
CPU_SMI#	AH41
CPU_PWRGD	AH43
CPU_RESET#	H38
CPU_SLP#	AM33
CPU_DPSP#	AN33
CPU_DPWR#	AG42
CPU_STPCLK#	AG42
CPU_DPRSTP#	AN32



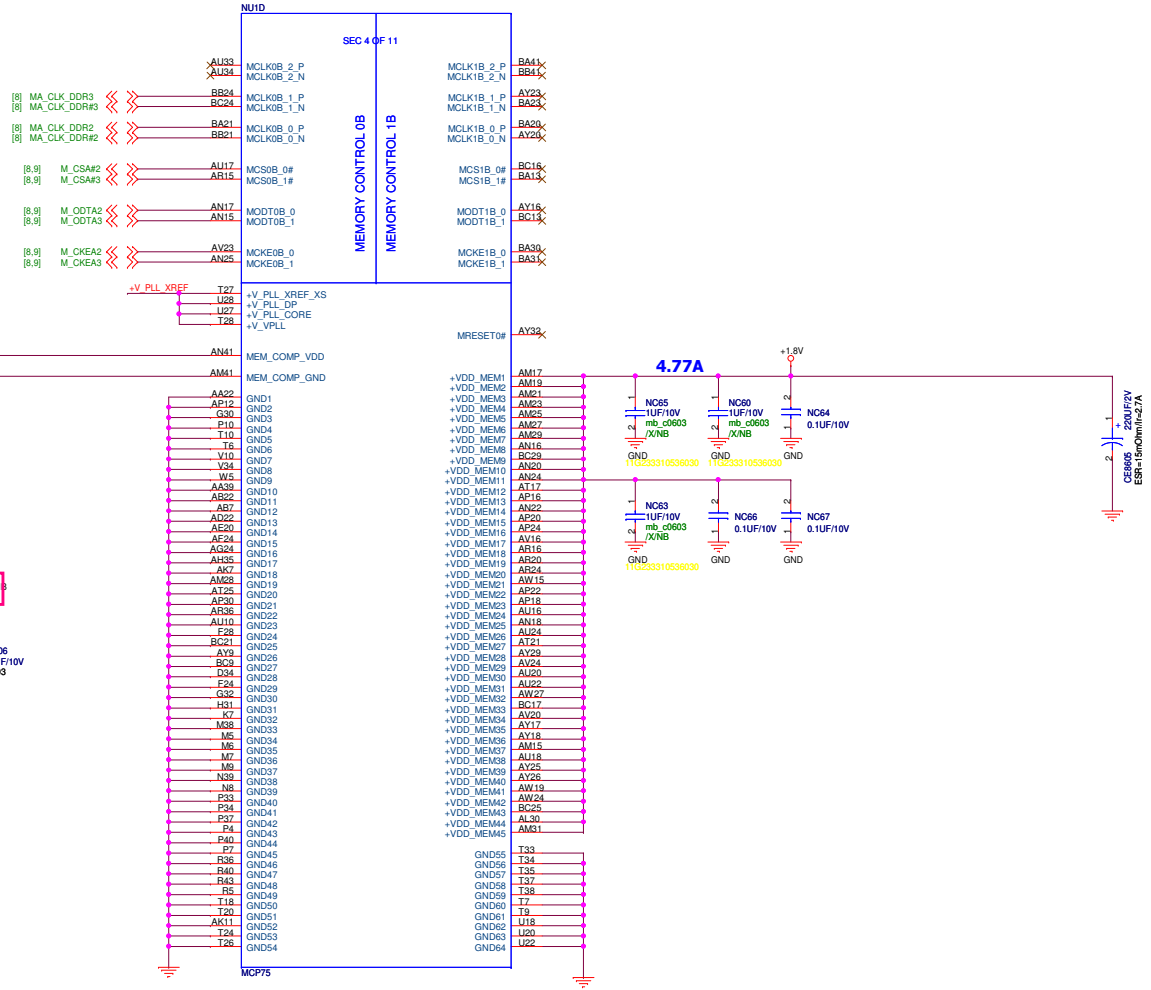
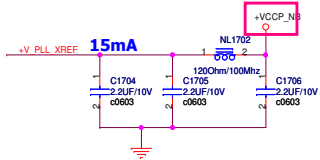
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	0
200	800	0	1	0
266	1067	0	0	0

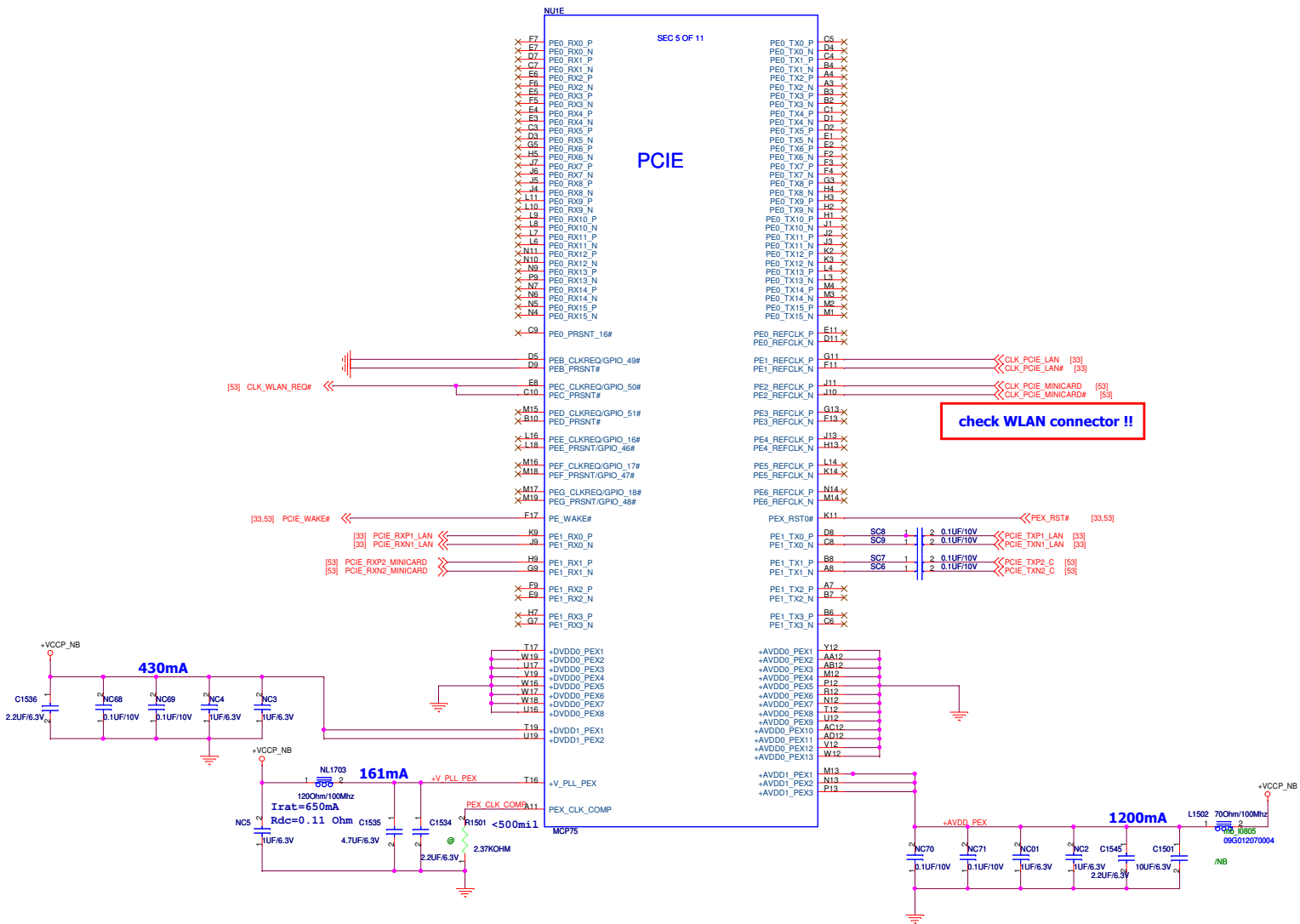






REF: DG-03328-001_V03





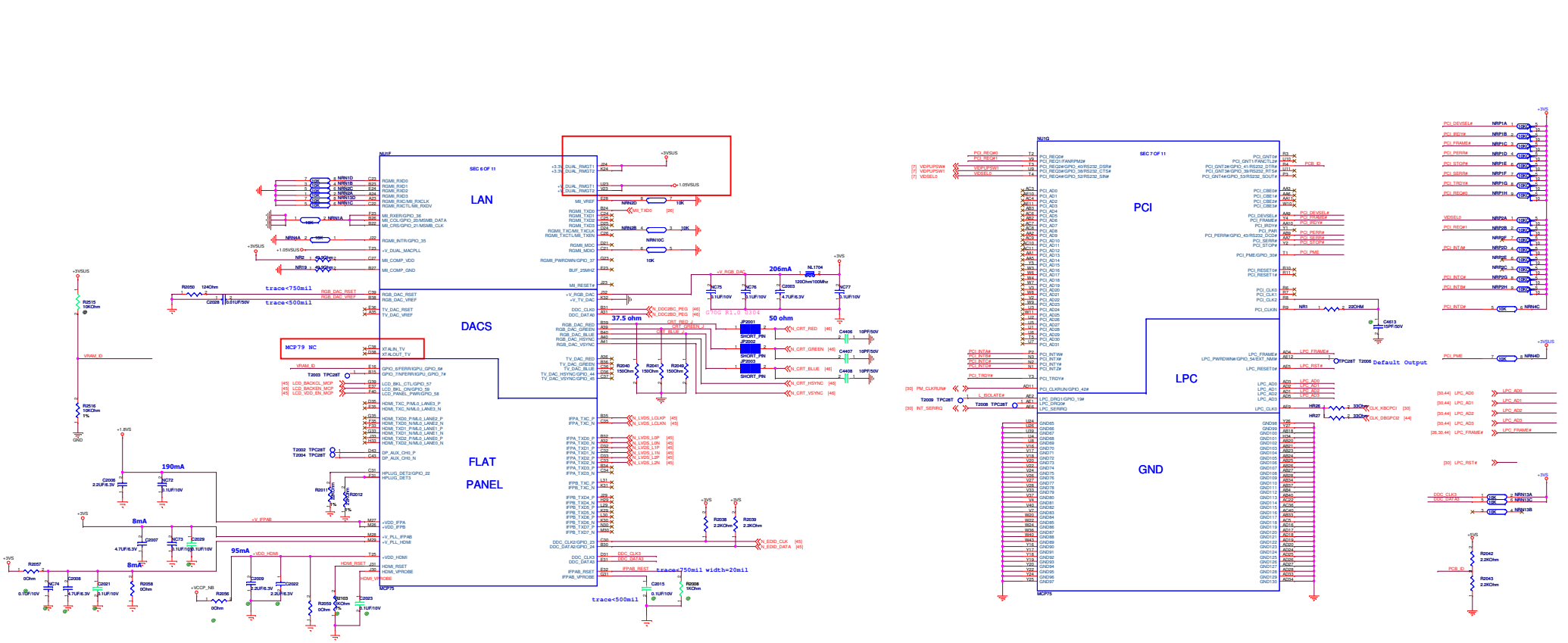
<Variant Name>



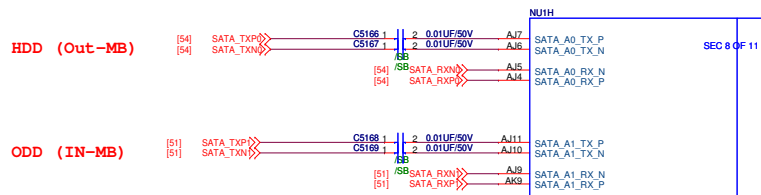
Title : SB-ICH9M(1)

Engineer:

Size	Project Name	Rev
C		1.0



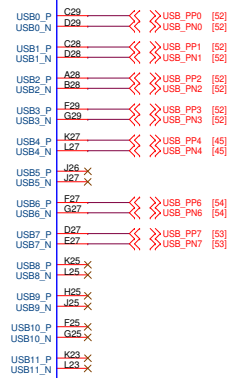
Check connector pin definition !!



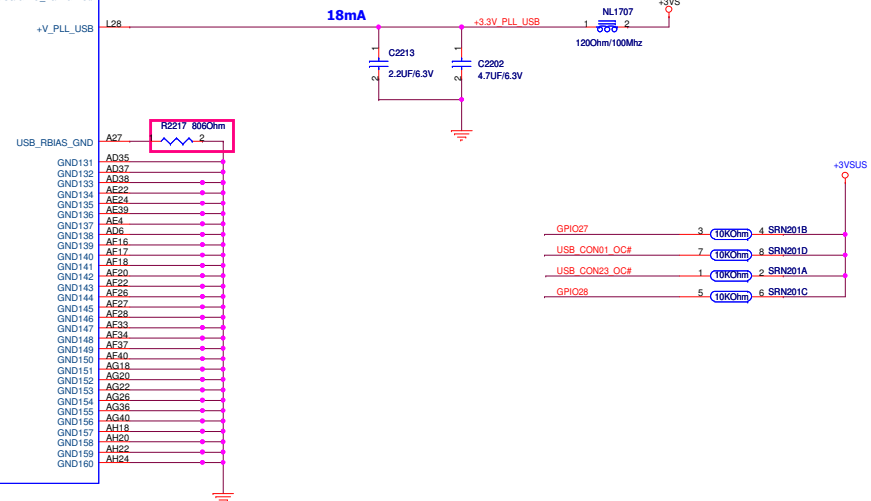
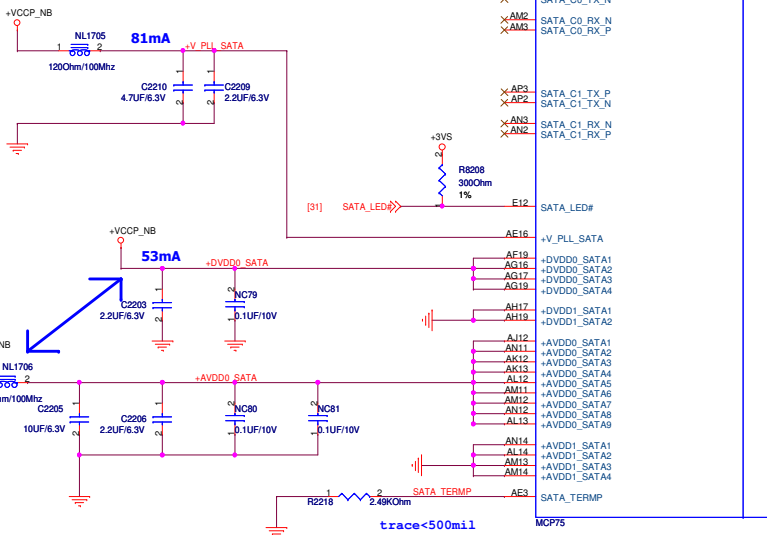
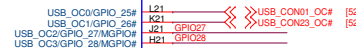
SATA

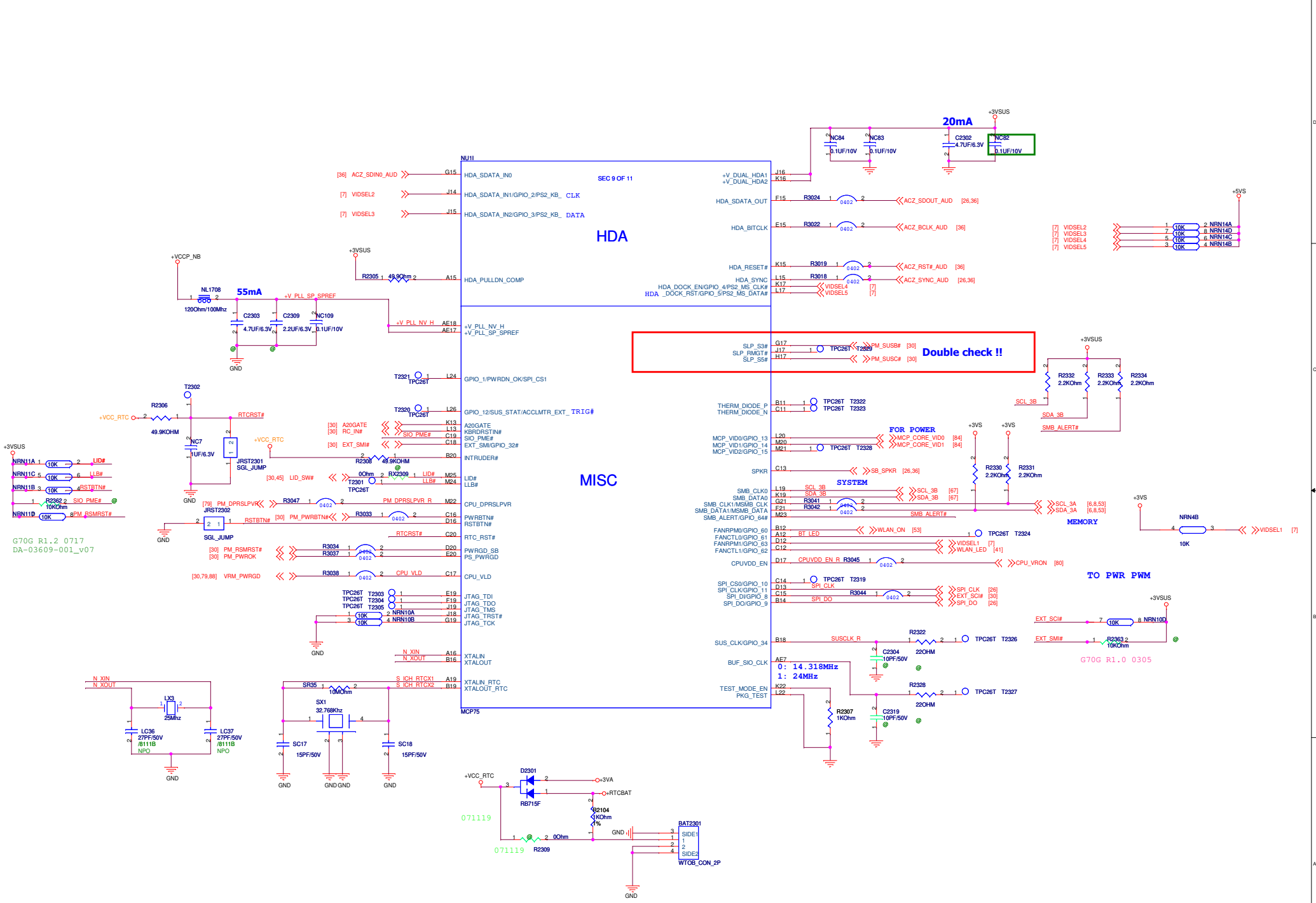
USB

Check connector pin definition !!

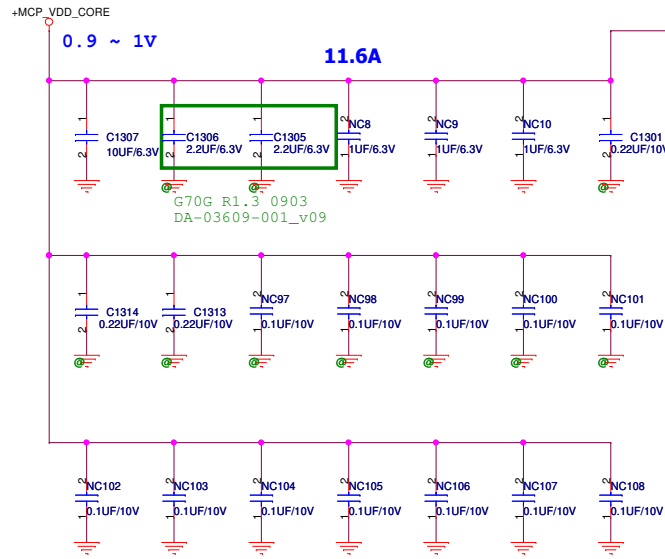


USB0	External Port 1
USB1	External Port 2
USB2	External Port 3
USB3	External Port 4
USB4	CMOS Camera
USB5	
USB6	CardReader
USB7	WiFi
USB8	
USB9	
USB10	
USB11	Finger Printer(Reserve)



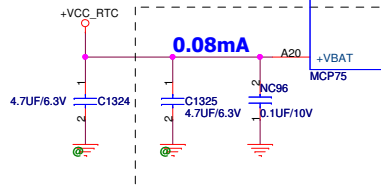


G70G R1.2 0717
DA-03609-001_v07

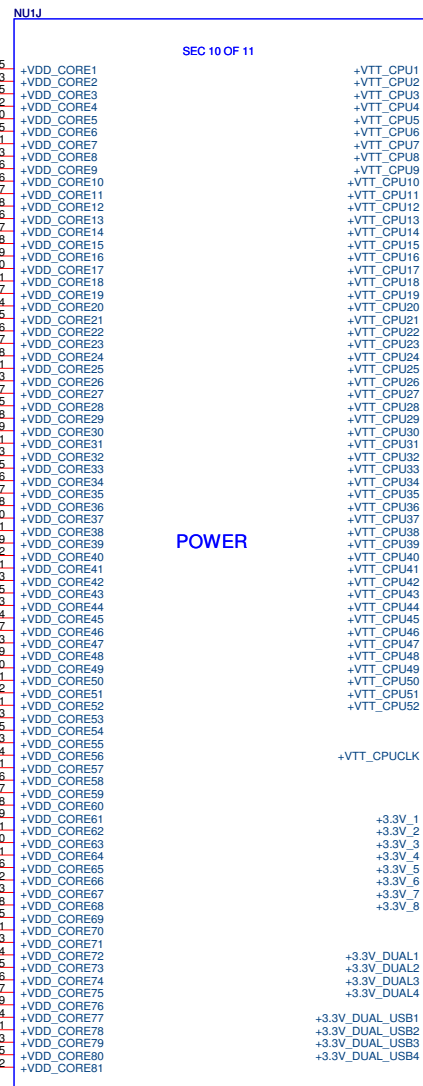


+MCP_VDD_VCORE

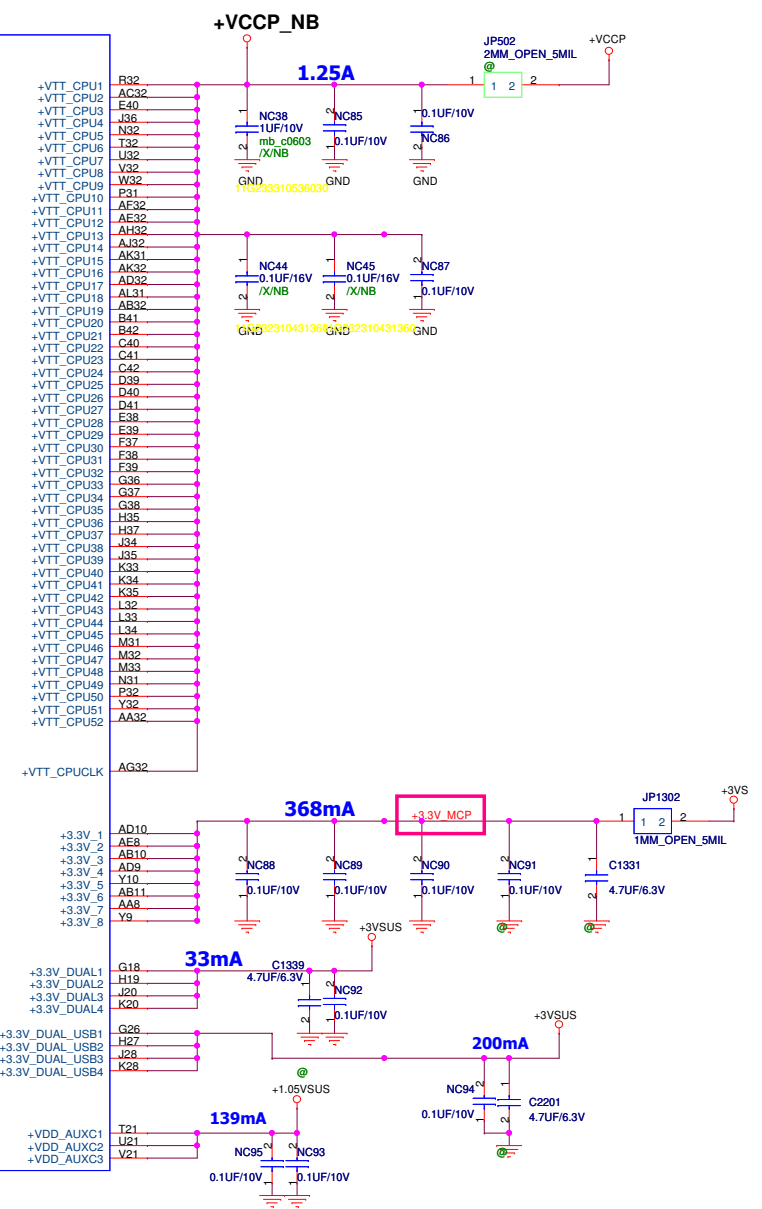
+MCP_VDD_VID[2:0]	Core Voltage
001	1
010	0.95
011	0.9



REF:DG-03328-001_V03



POWER



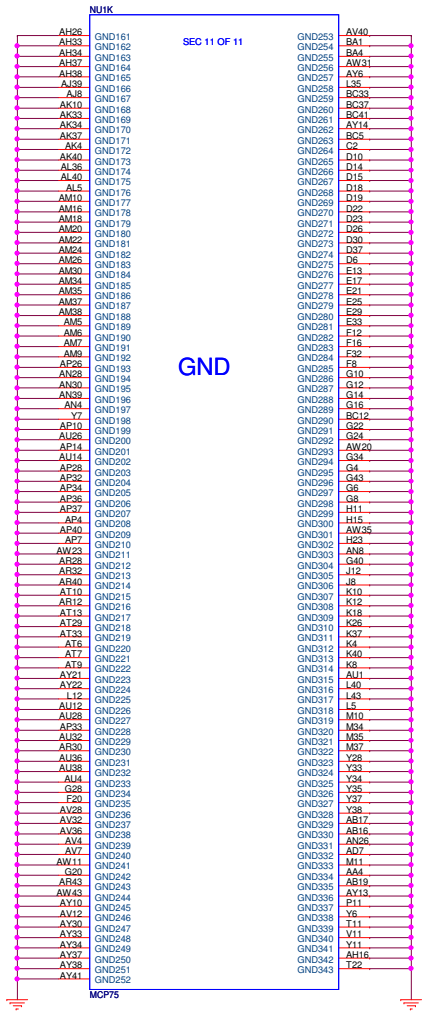
<Variant Name>

ASUS Title : ICH9M-Other

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 24 of 91



<Variant Name>

		Title : SPI ROM
Engineer:		
Size	Project Name	Rev
C		1.0
Date: Friday, February 13, 2009		Sheet 25 of 91

[6.8.23.53] SCL_3A << >> SMB_CLK_S [6.8.23.53]

[6.8.23.53] SDA_3A << >> SMB_DAT_S [6.8.23.53]

Onboard DRAM ID

GPIO_6	GPIO_11	Vendor
0	0	Qimonda HYB187512161B2F-25
0	1	Samsung K4N51163Q2-HC25
1	0	Hynix HY5FS121621CFP-25

HDA_SYNC STRAP (BUF_SIO_CLK)

0	14.318MHz (default)
1	24MHz

RGMIITXDO

0	MII
1	RGMIITXDO

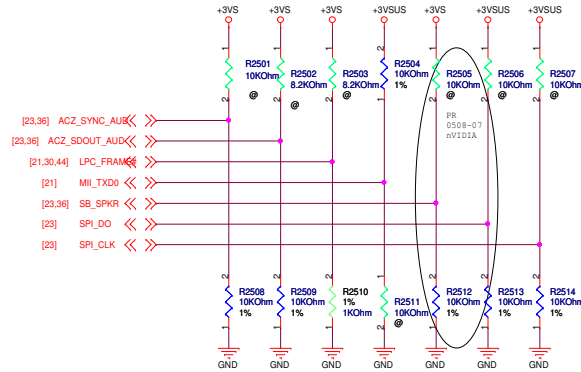
SPKR

0	User mode boot Init table
1	Safe mode boot Init table

Base on EC

HDA_SDOUT	LPC_FRAME	FUNCTION
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS

SPI_DO	SPI_CLK	FUNCTION
0	0	31MHz
0	1	42MHz
1	0	25MHz
1	1	1MHz



<Variant Name>

ASUS		Title :
		Engineer:
Size	Project Name	Rev
C		1.0
Date:	Monday, February 16, 2009	Sheet 26 of 91

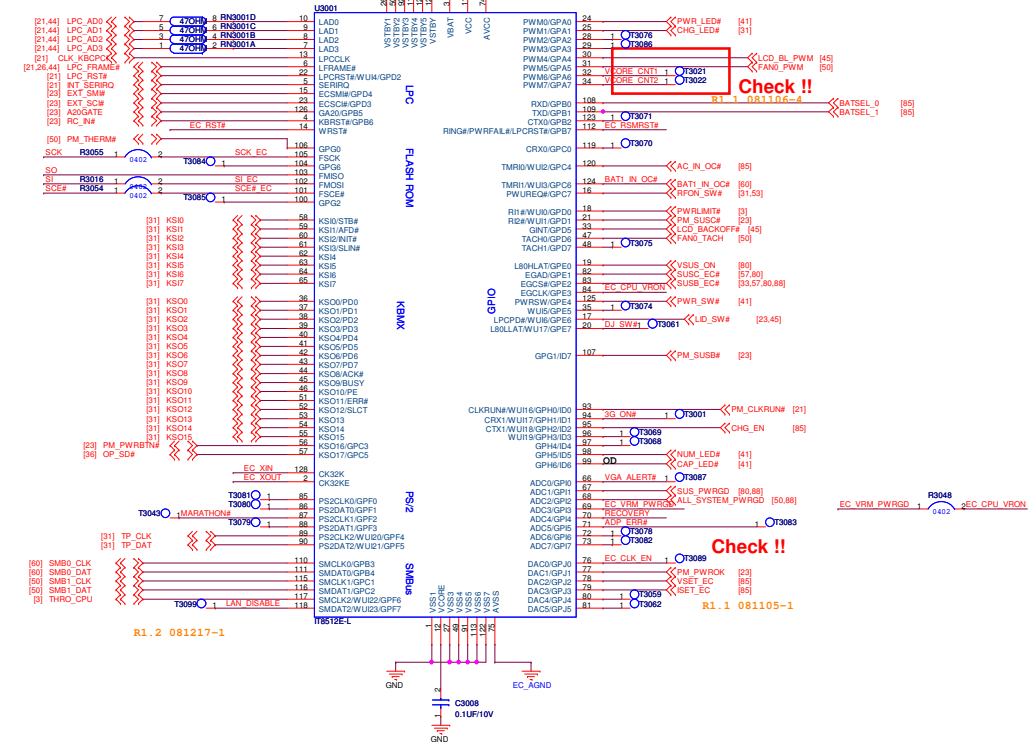
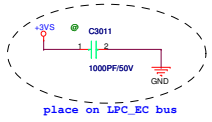


<Variant Name>

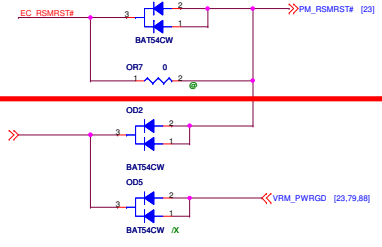
		Title :
ASUSTeK COMPUTER INC. NB6		Engineer: Vincent Chung
Size	Project Name	Rev
C	G71V	1.0
Date: Friday, February 13, 2009		Sheet 27 of 91

<Variant Name>

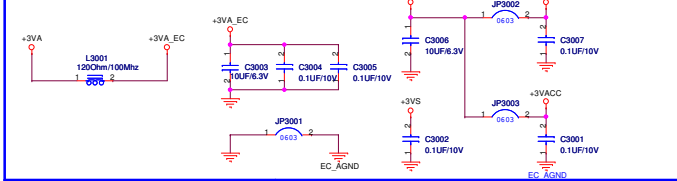
		Title : Main Clock-2
ASUS Tek Computer Inc.		Engineer: Tony Kao
Size	Project Name	Rev
A2	C90P	1.00
Date: Friday, February 13, 2009		Sheet 29 of 91



2.0G-G71G STUFF OD1



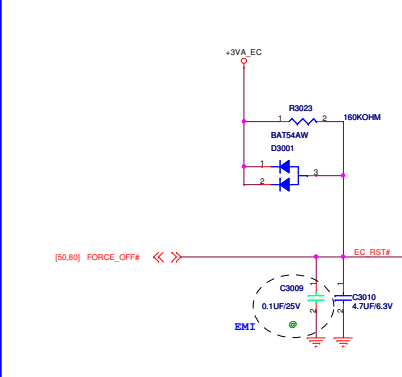
For IT8752 Power



For PU / PD



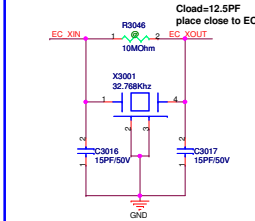
For EC Reset



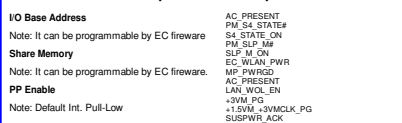
For Instant Key



For X'tal



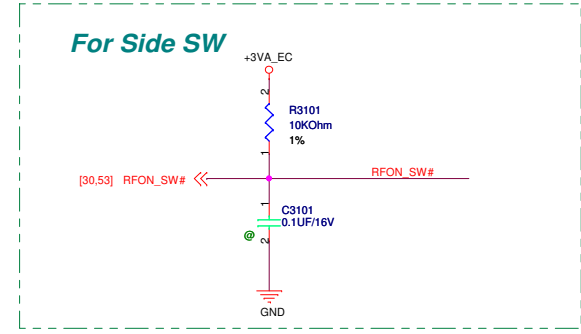
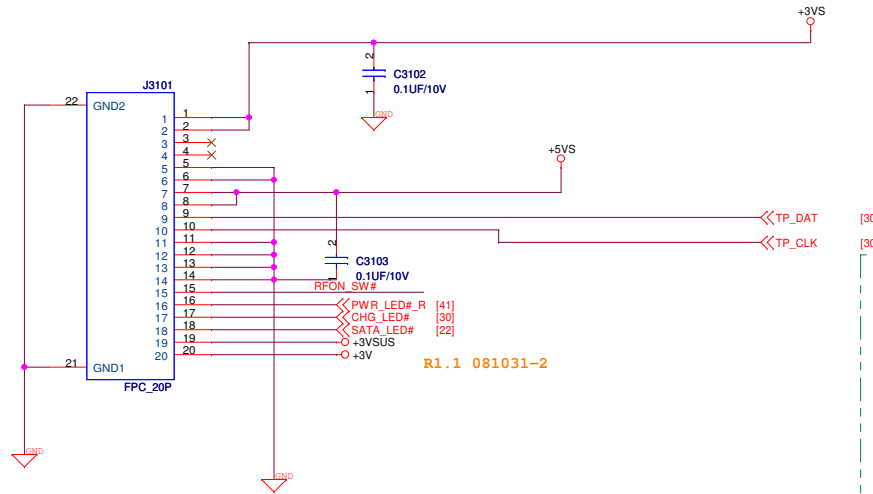
For EC Hardware Strap



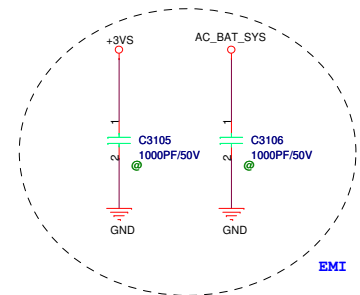
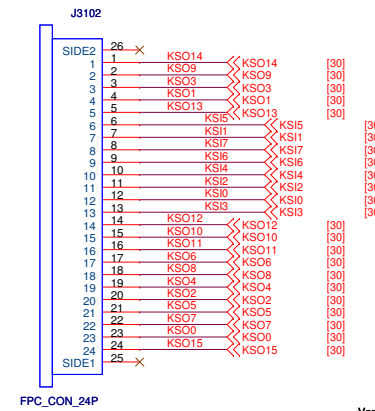
For iAMT pin name

I/O Base Address	AC_PRESENT
Note: It can be programmable by EC firmware	PM_S4_STATE#
Share Memory	S4_STATE_ON
Note: It can be programmable by EC firmware.	PM_SLP_M#
PP Enable	SLP_M_ON
Note: Default Int. Pull-Low	EC_WLAN_PWR
	MP_PWRCD
	AC_PRESENT
	LAN_WOL_EN
	+3VM_PG
	+1.5VM_3VMCLK_PG
	SUSPWR_ACK

TouchPad & FingerPrint



Keyboard Connector




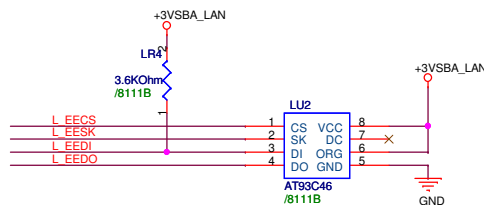
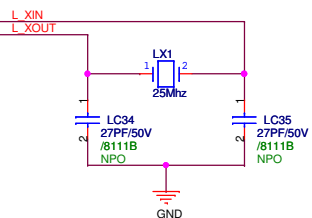
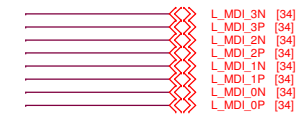
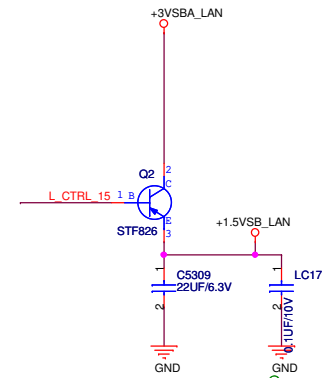
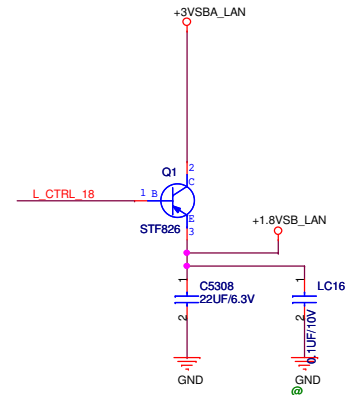
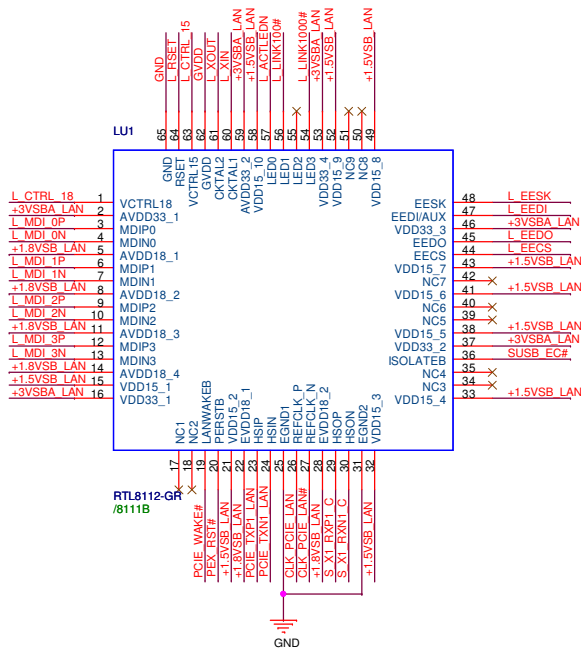
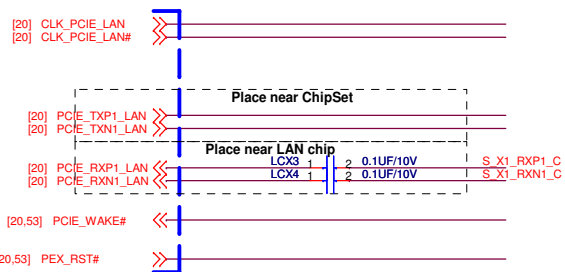
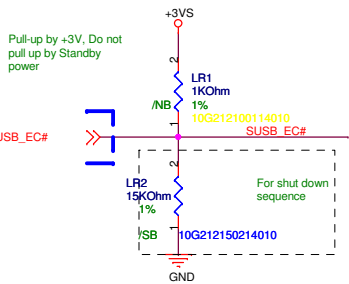
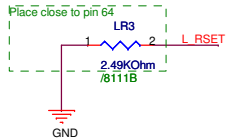
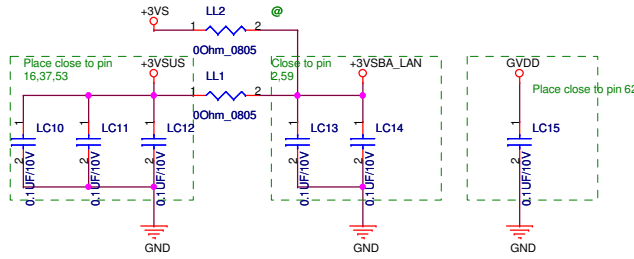
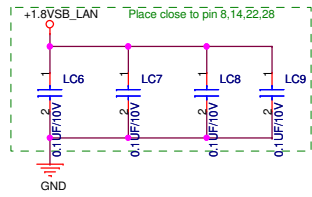
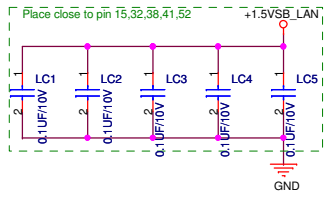
For Thermal Control Method

Remove redundant components



<Variant Name>

		Title : RST_Reset Circuit
ASUSTeK COMPUTER INC. NB1		Engineer: Vincent Chung
Size	Project Name	Rev
Custom	G71V	1.0
Date: Friday, February 13, 2009		Sheet 32 of 91



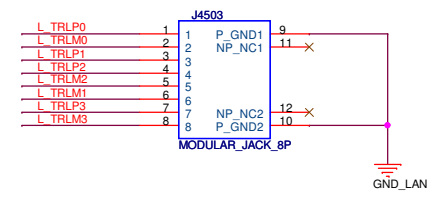
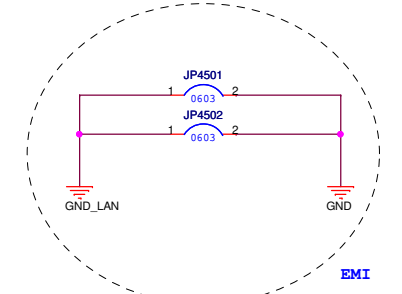
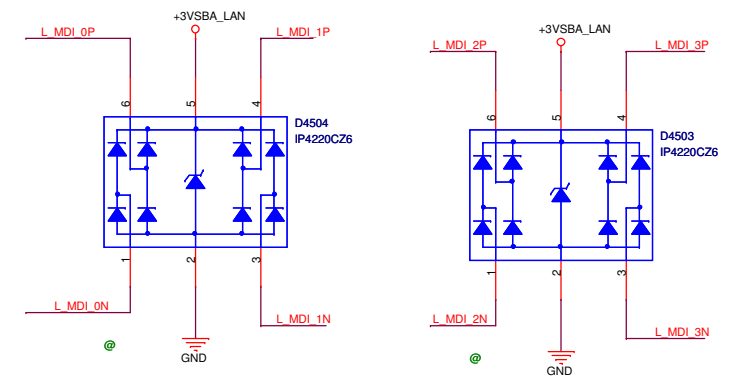
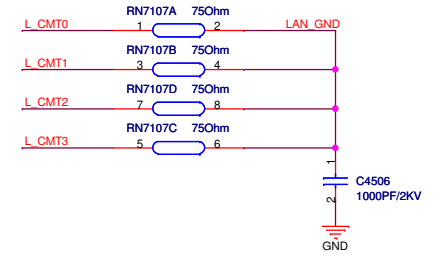
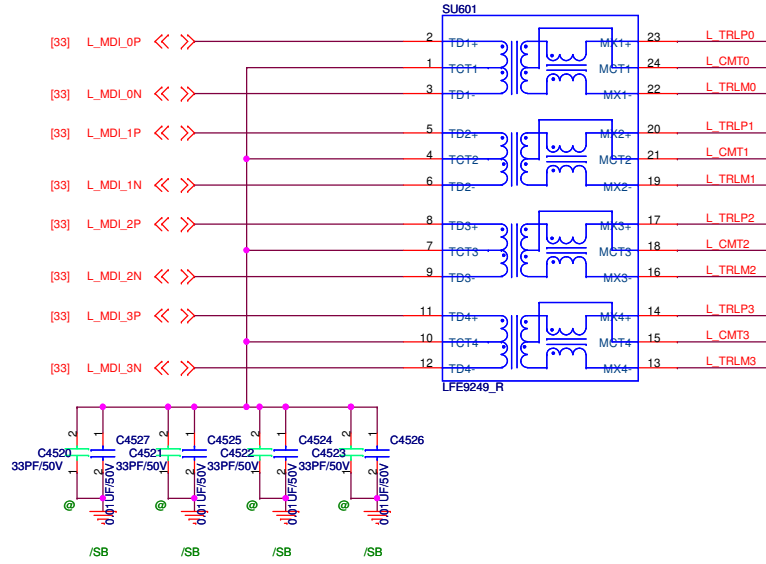
<Variant Name>

Title : RST_Reset Circuit
ASUSTek COMPUTER INC. NB1
Engineer: Vincent Chung

Size	Project Name	Rev
Custom	G71V	1.0

Date: Friday, February 13, 2009 Sheet 33 of 91

LAN CONN.



<Variant Name>

ASUS Title : 10


ASUSTeK COMPUTER INC Engineer:

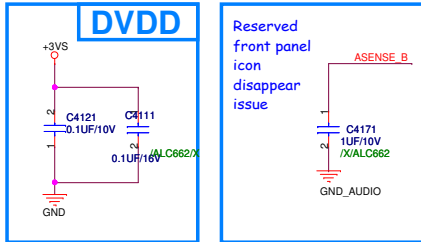
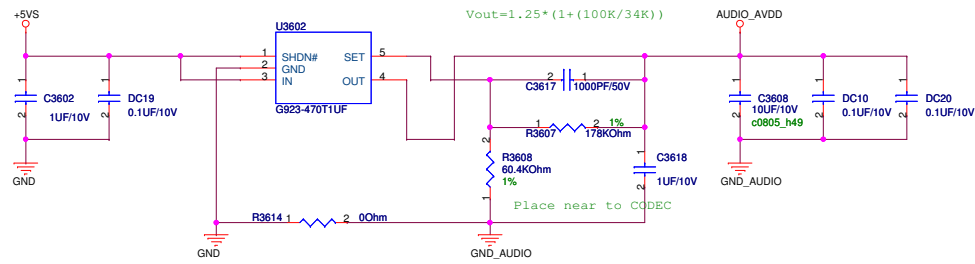
Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 34 of 91

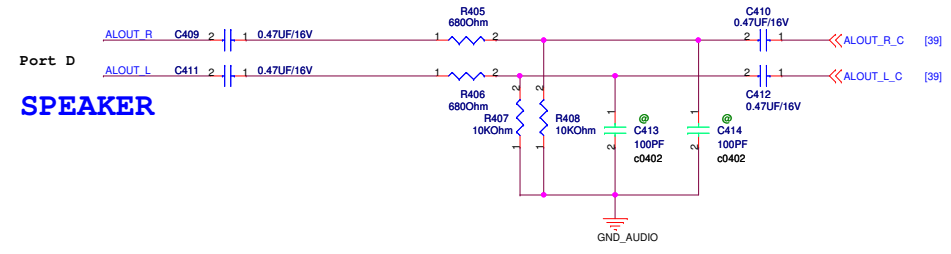
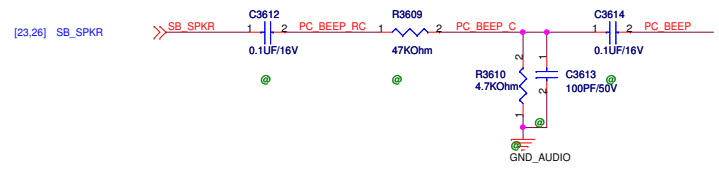
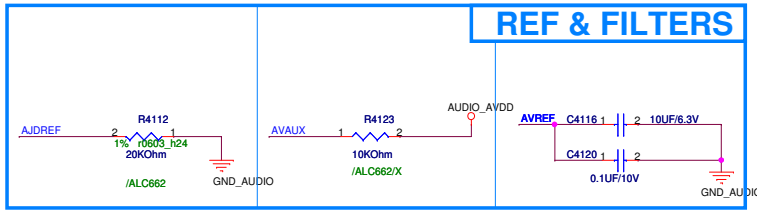
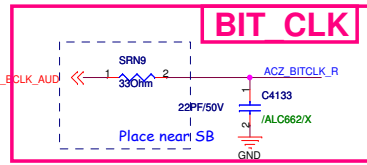
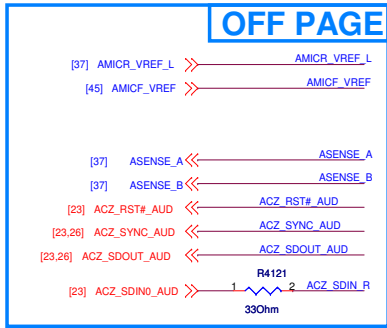
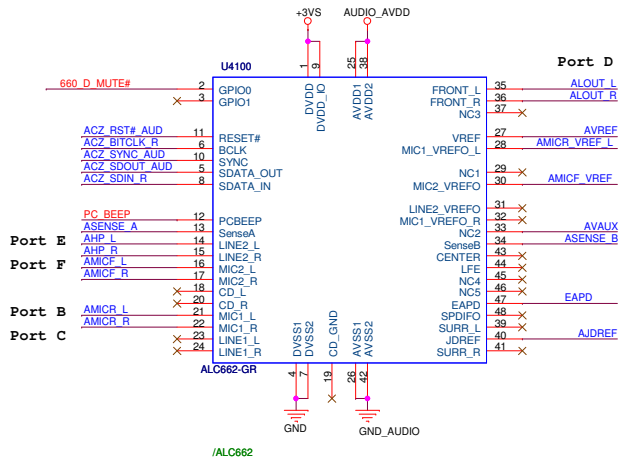


<Variant Name>

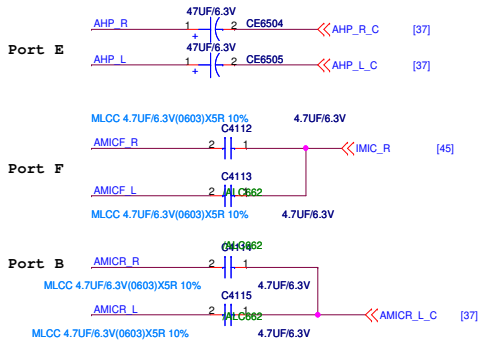
		Title : MDC
ASUSTeK COMPUTER INC		Engineer: <i>Vincent Chung</i>
Size	Project Name	Rev
Custom	G71V	1.0
Date: Friday, February 13, 2009		Sheet 35 of 91



CODEC ALC662

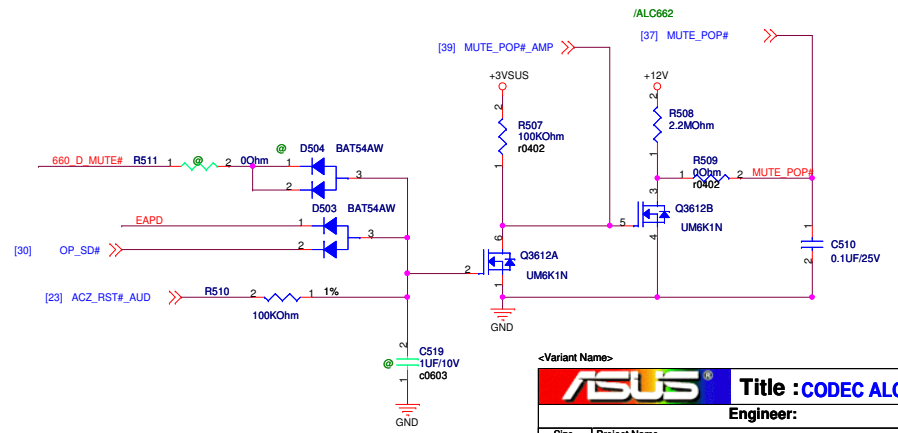


HP CONN



Internal Mic

External Mic



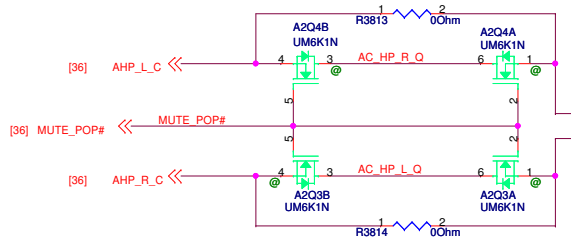
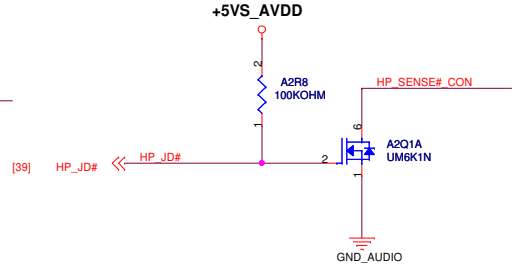
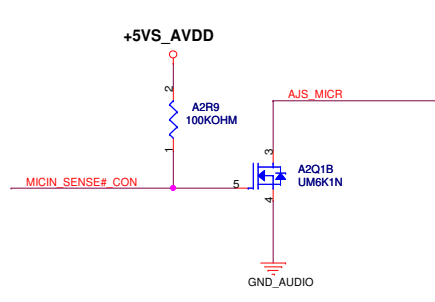
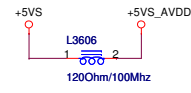
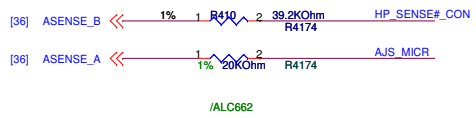
<Variant Name>

Title : CODEC ALC662

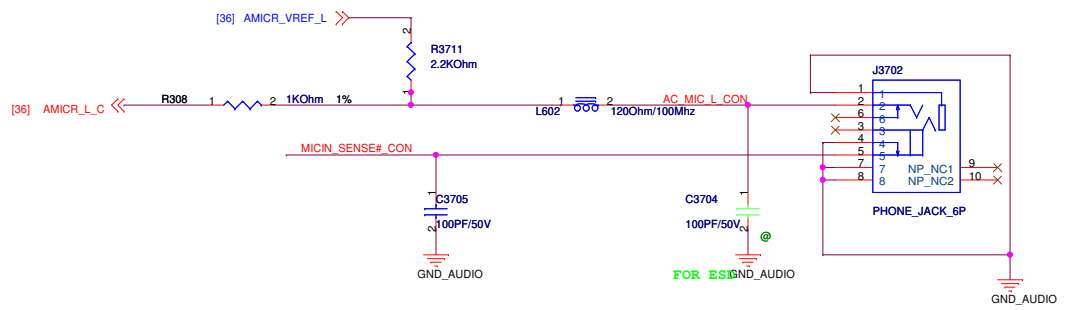
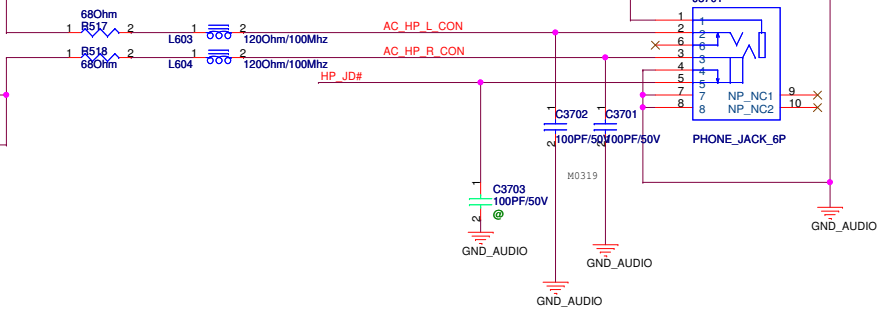
Engineer:

Size	Project Name	Rev
Custom		1.1

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HP CONN

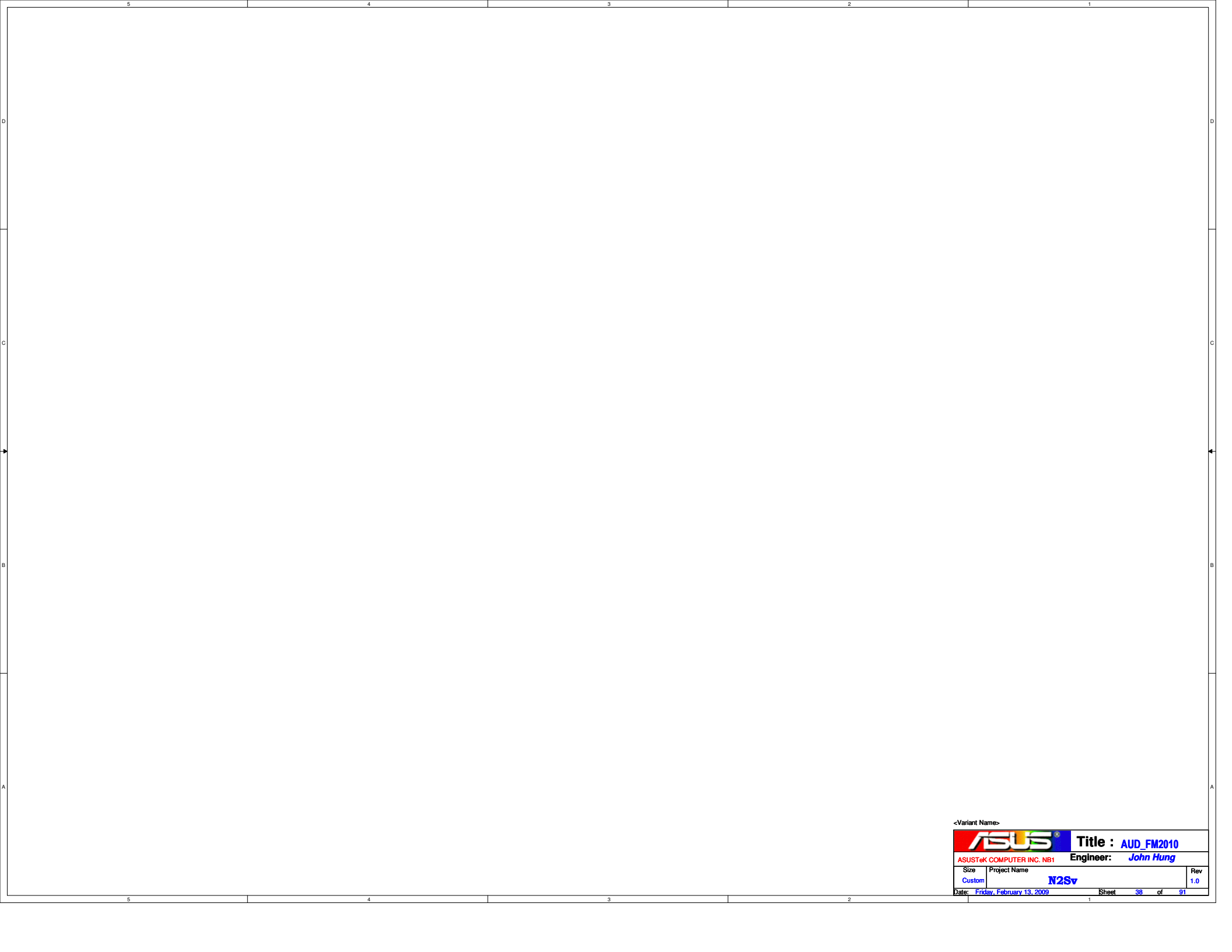


External MIC CONN

<Variant Name>

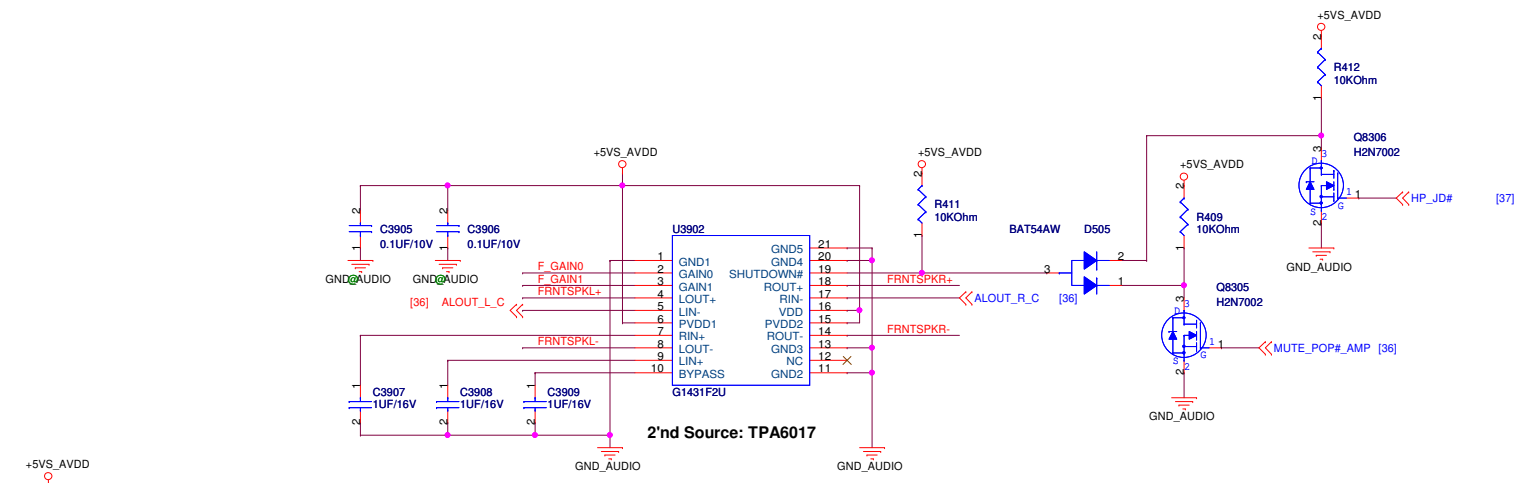
ASUS Title : **AUD_Amp & Jack**
 Engineer:

Size	Project Name	Rev
Custom		1.0
Date:	Friday, February 13, 2009	Sheet 37 of 91

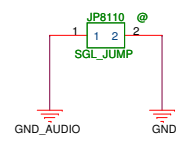
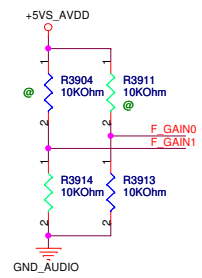


<Variant Name>

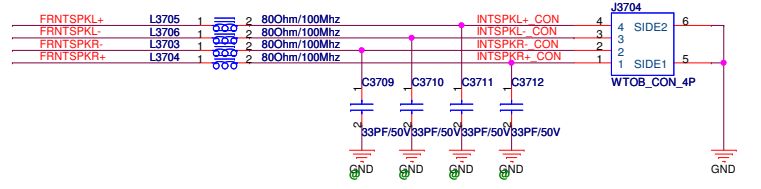
		Title : <i>AUD_FM2010</i>
ASUSTeK COMPUTER INC. NB1		Engineer: <i>John Hung</i>
Size Custom	Project Name N2Sv	Rev 1.0
Date: <i>Friday, February 13, 2009</i>		Sheet 38 of 91



2'nd Source: TPA6017

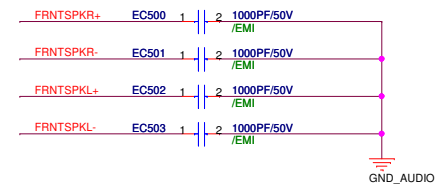


SPEAKER CONNECTOR (2W)



GAIN0	GAIN1	Av (irv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

2.0G-G71G-EMI

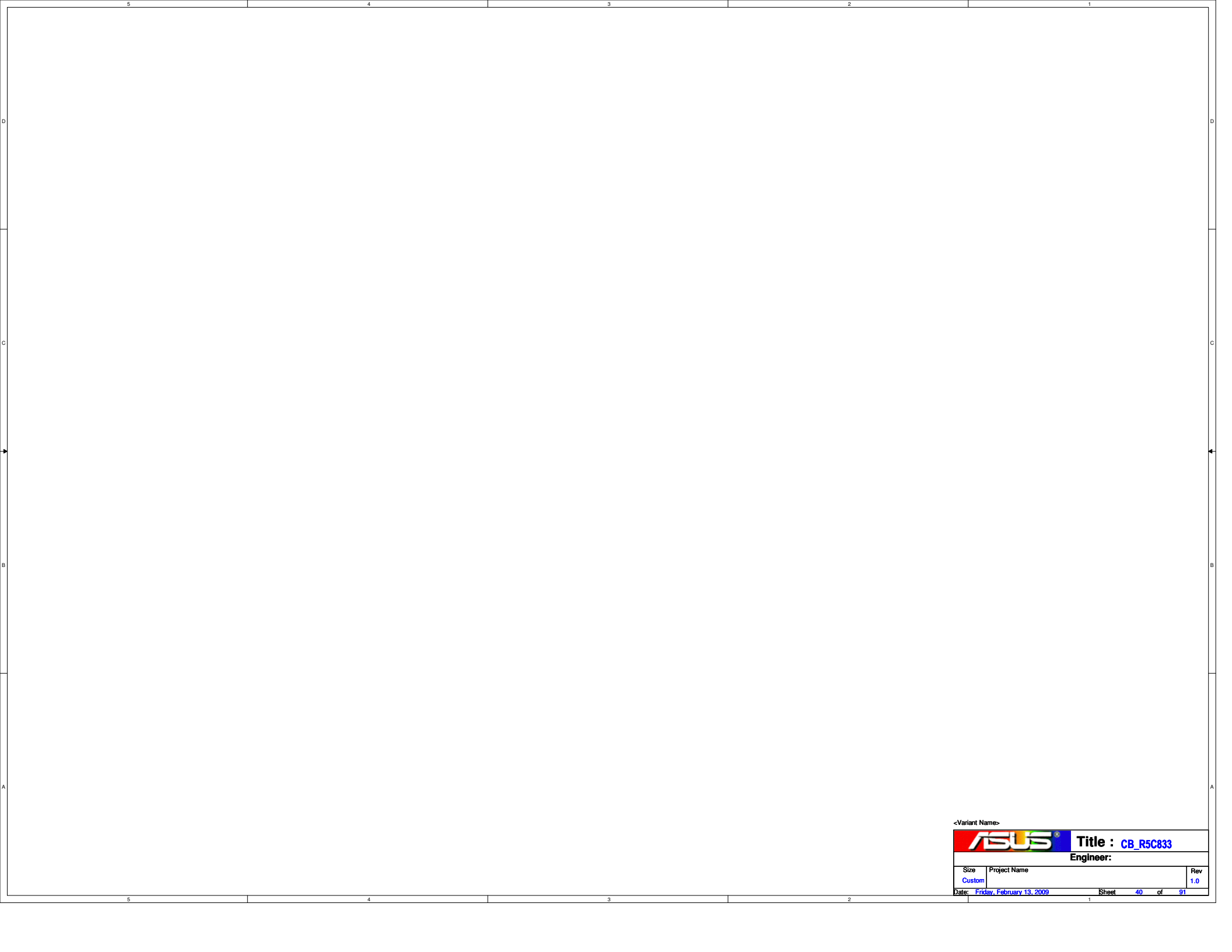


<Variant Name>


Title : AUD_Woofers & Front
Engineer:

Size	Project Name	Rev
Custom		1.0

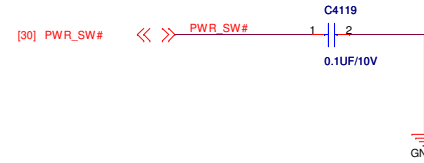
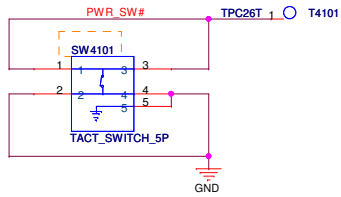
Date: Friday, February 13, 2009 Sheet 39 of 91



<Variant Name>

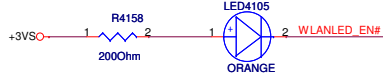
		Title : CB_R5C833
Engineer:		
Size	Project Name	Rev
Custom		1.0
Date: Friday, February 13, 2009	Sheet	40 of 91

SWITCH BUTTON

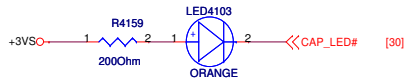


LED

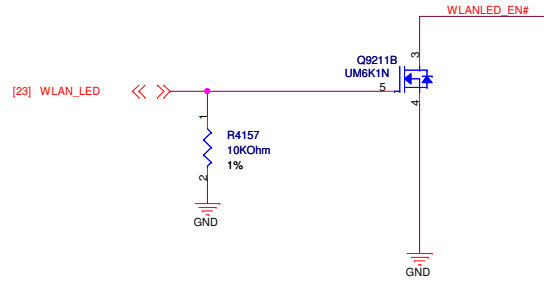
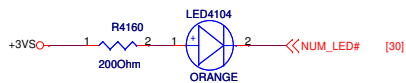
For WireLess LED



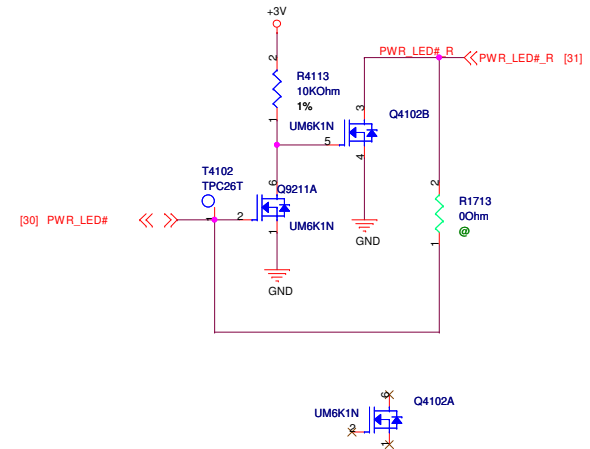
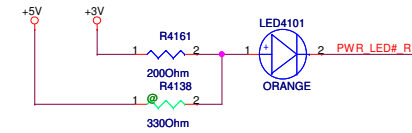
for Cap. Lock



for Num Lock

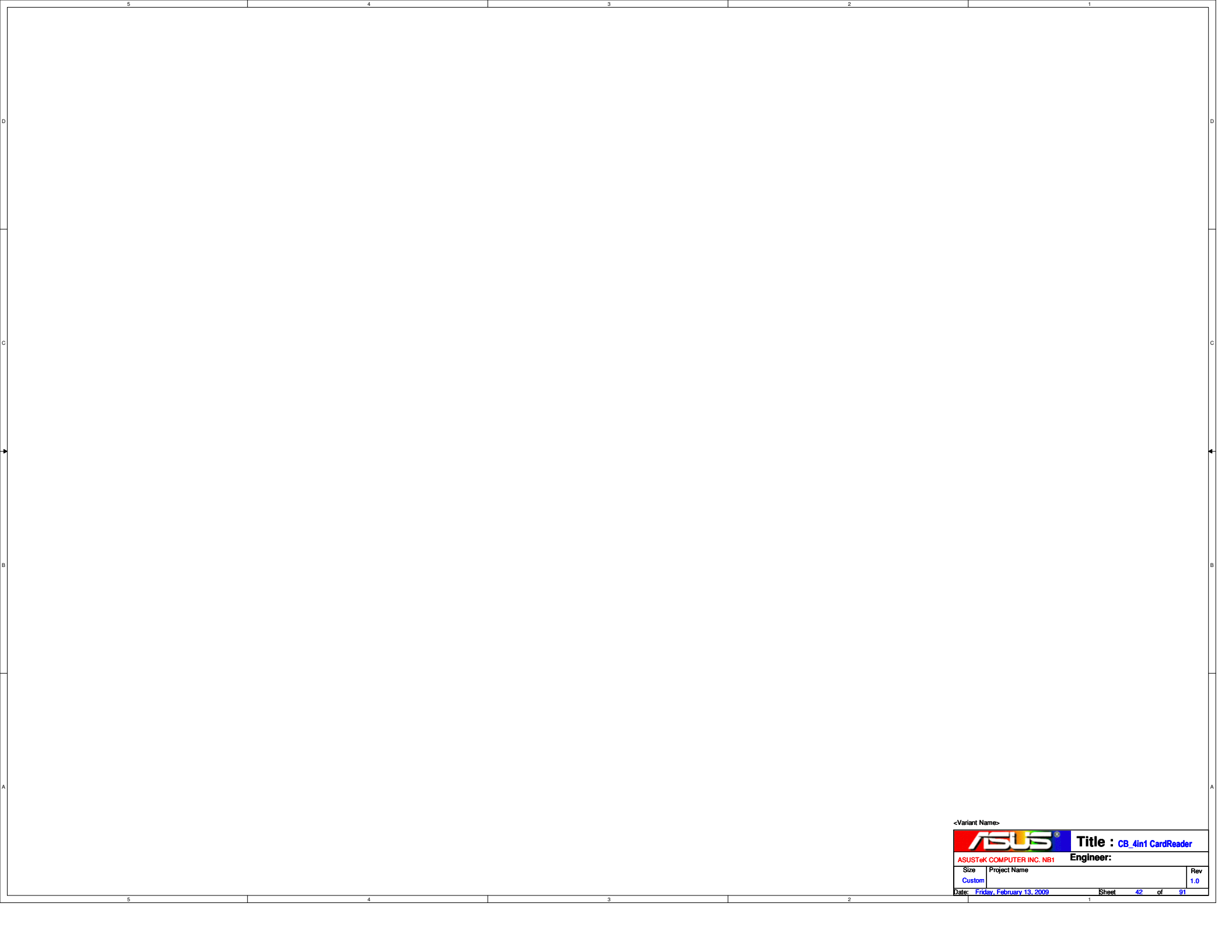


For POWER LED




<Variant Name>

ASUS		Title : CB_R5C833	
ASUSTeK COMPUTER INC. NB1		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Friday, February 13, 2009	Sheet	41	of 91



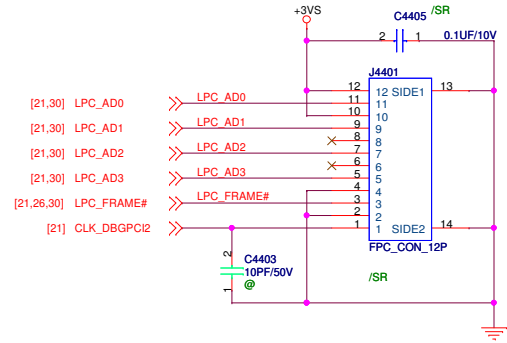
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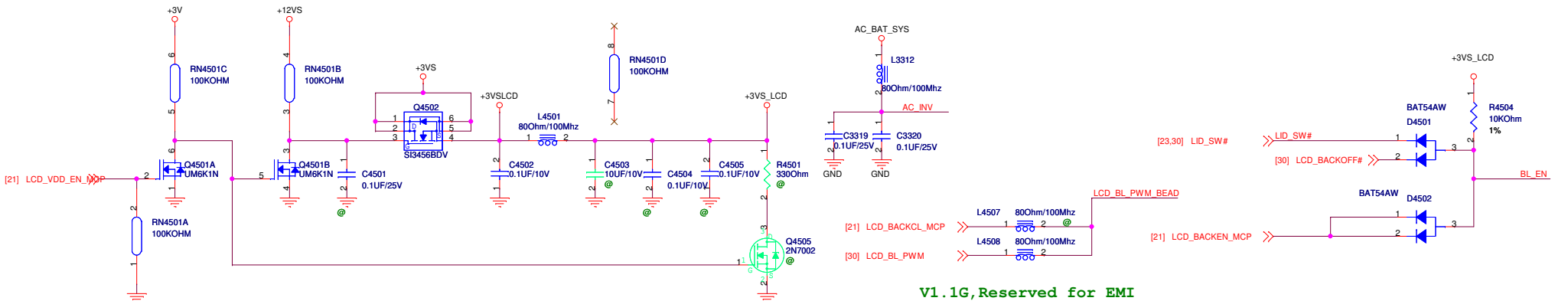
		Title : CB_4in1 CardReader
ASUSTeK COMPUTER INC. NB1		Engineer:
Size	Project Name	Rev
Custom		1.0
Date:	Friday, February 13, 2009	Sheet 42 of 91



-Variant Name-

		Title : NEW CARD
Engineer:		
Size	Project Name	Rev
Custom		1.1
Date: Friday, February 13, 2009		Sheet 43 of 91

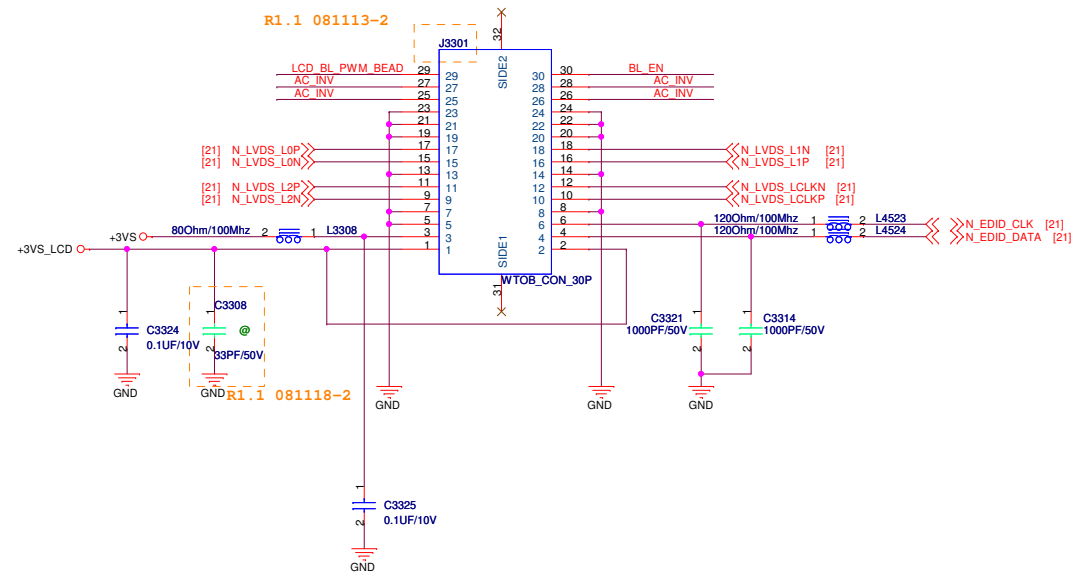




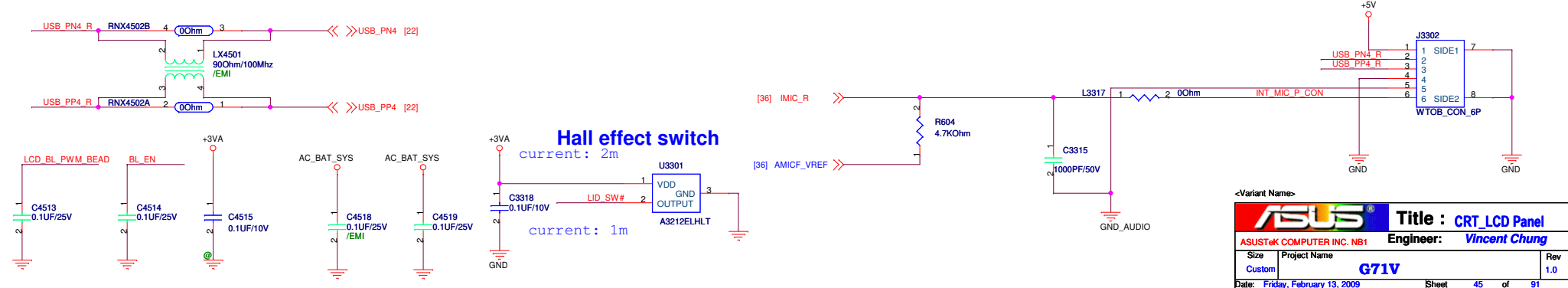
LED PANEL LVDS Interface

R1.1 081113-2
R1.2 081202-1

V1.1G, Reserved for EMI

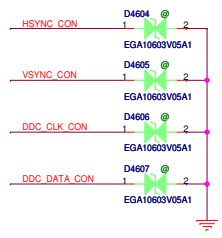
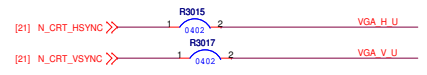
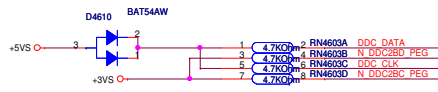
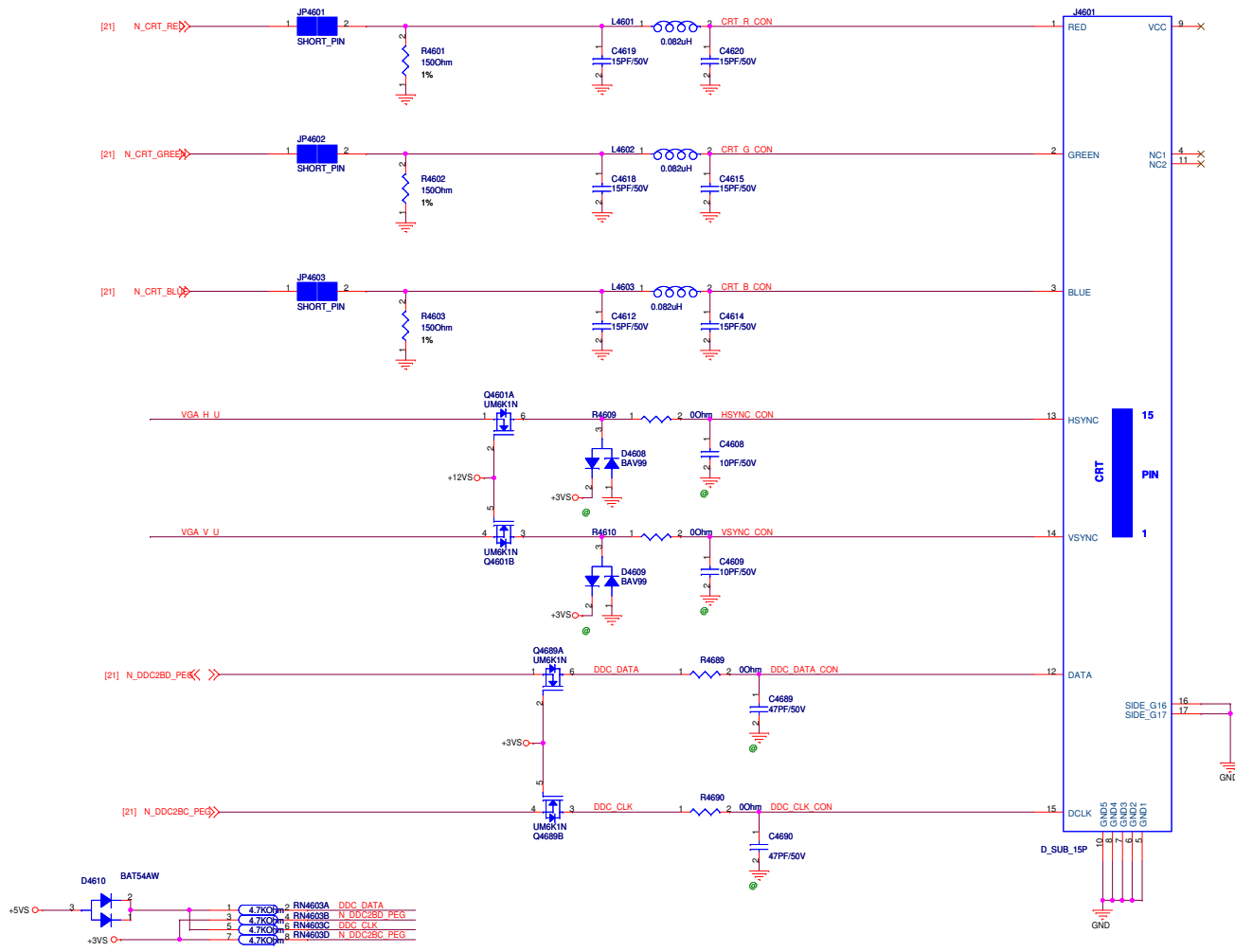


CAMERA & MIC

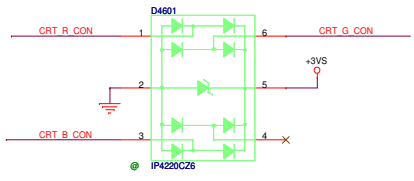


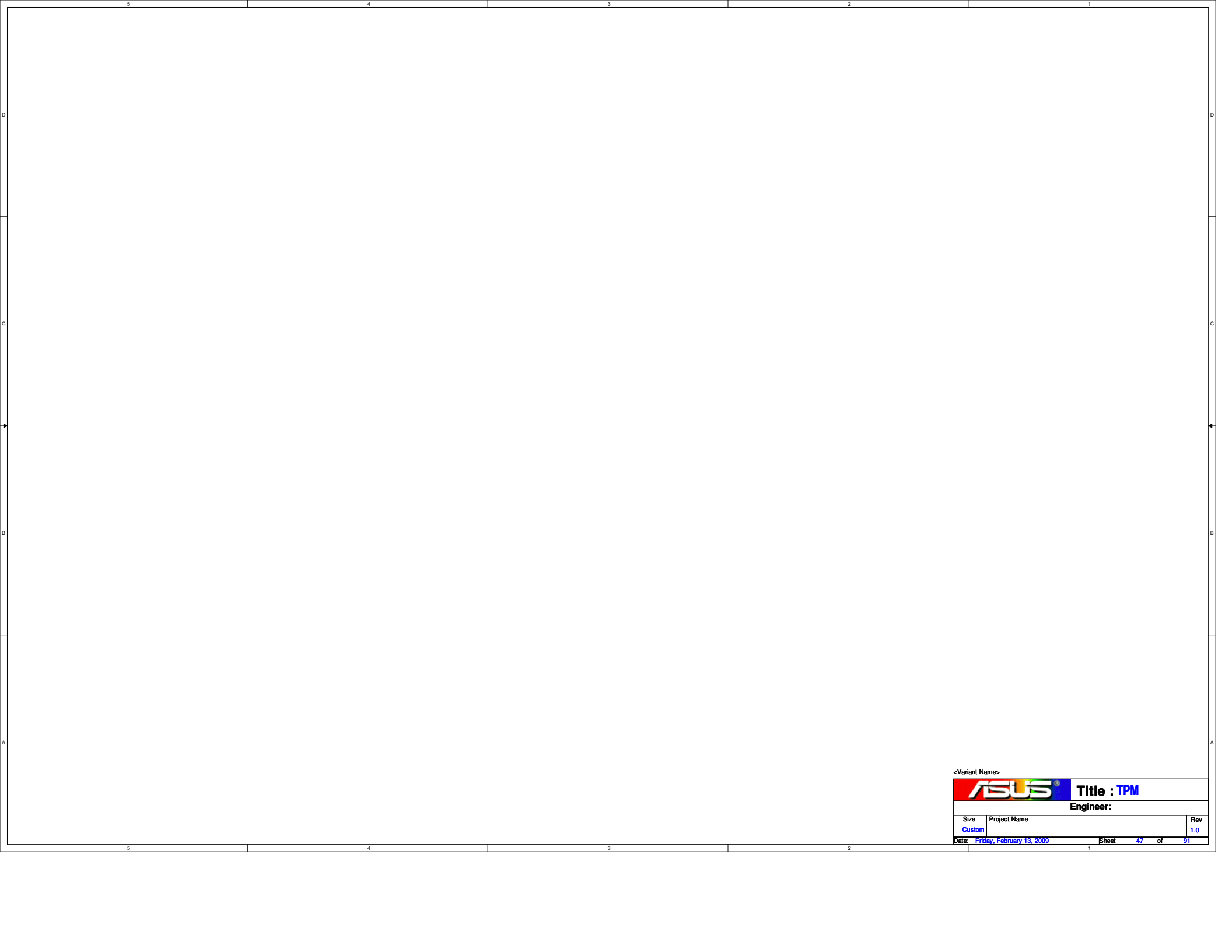
<Variant Name>

ASUS		Title : CRT_LCD Panel
ASUSTeK COMPUTER INC. NBI		Engineer: Vincent Chung
Size	Project Name	Rev
Custom	G71V	1.0
Date: Friday, February 13, 2009	Sheet	45 of 91




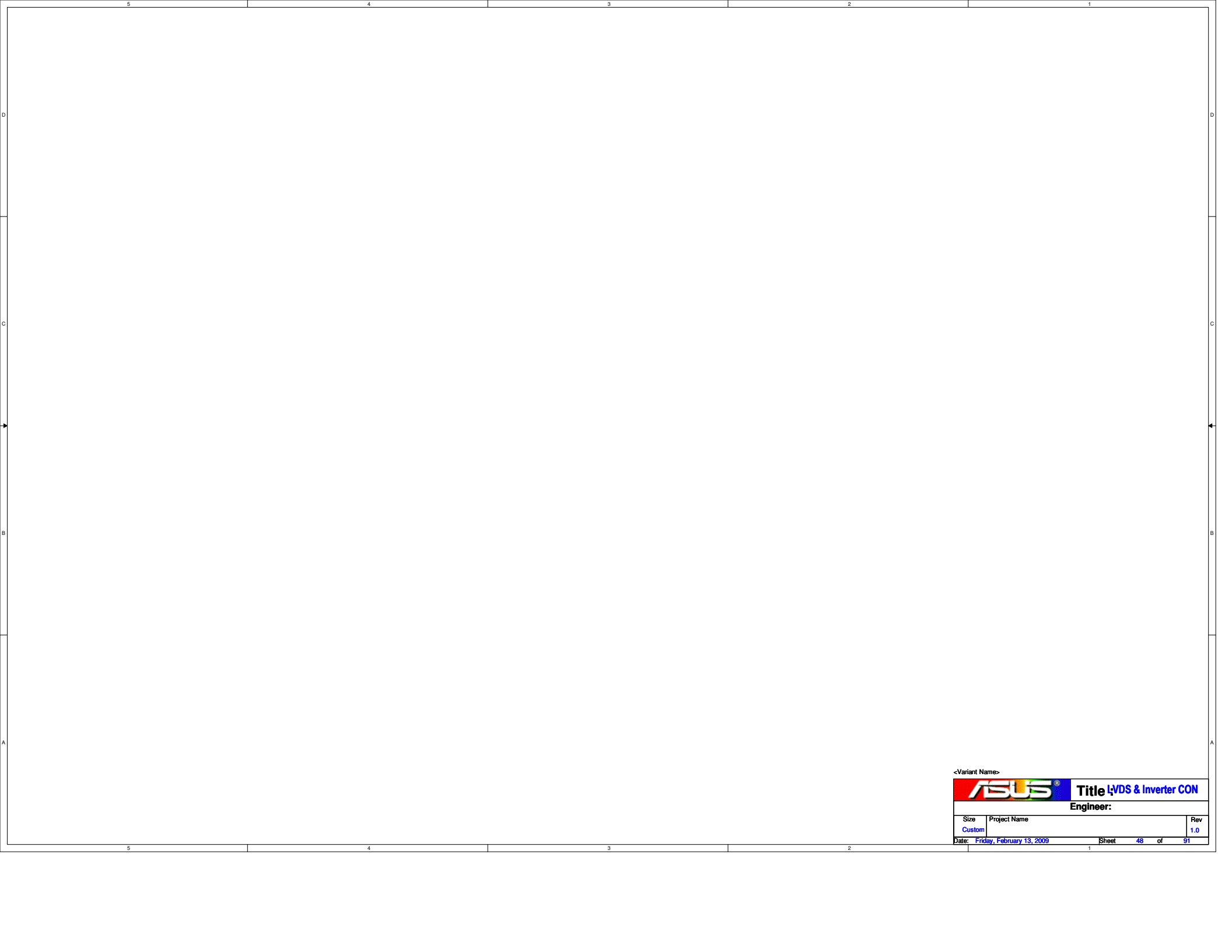
PLACE ESD Diodes near VGA port






-Variant Name-

		Title : TPM
Engineer:		
Size	Project Name	Rev
Custom		1.0
Date: Friday, February 13, 2009	Sheet	47 of 91



-Variant Name-

		Title LVDS & Inverter CON
Engineer:		
Size	Project Name	Rev
Custom		1.0
Date: Friday, February 13, 2009	Sheet 48 of 91	

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title :

Engineer:

Size A	Project Name	Rev 1.0
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5

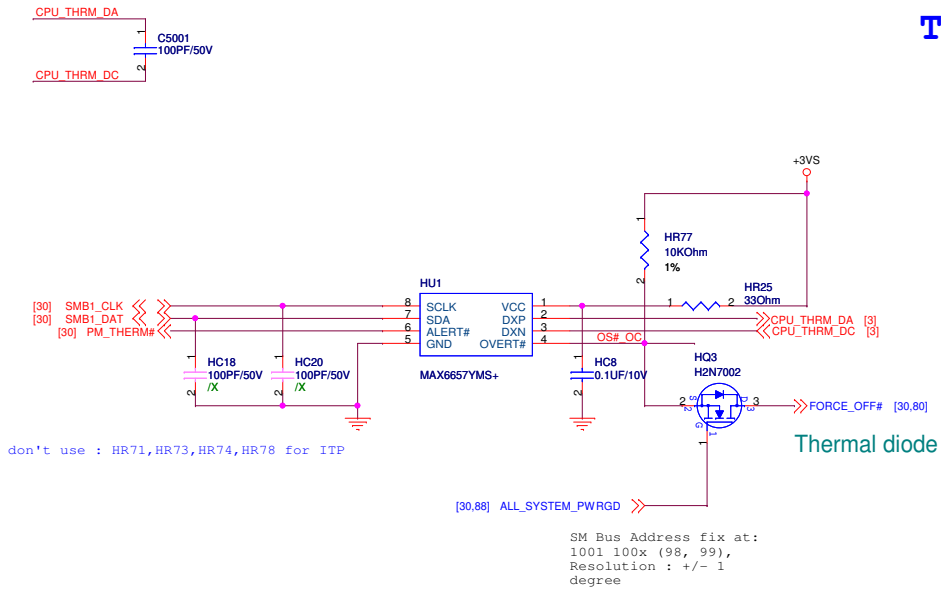
4

3

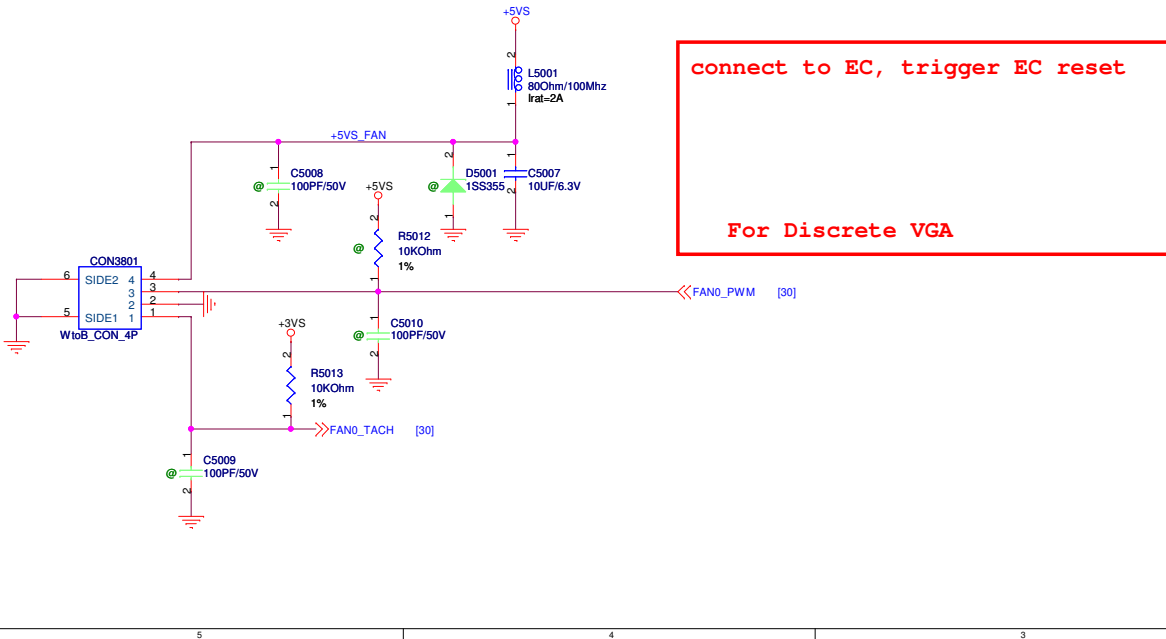
2

1

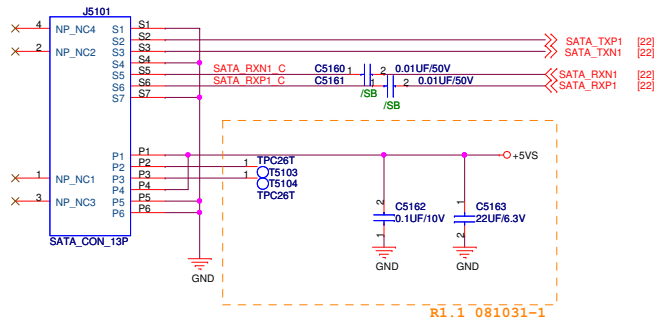
Thermal Sensor



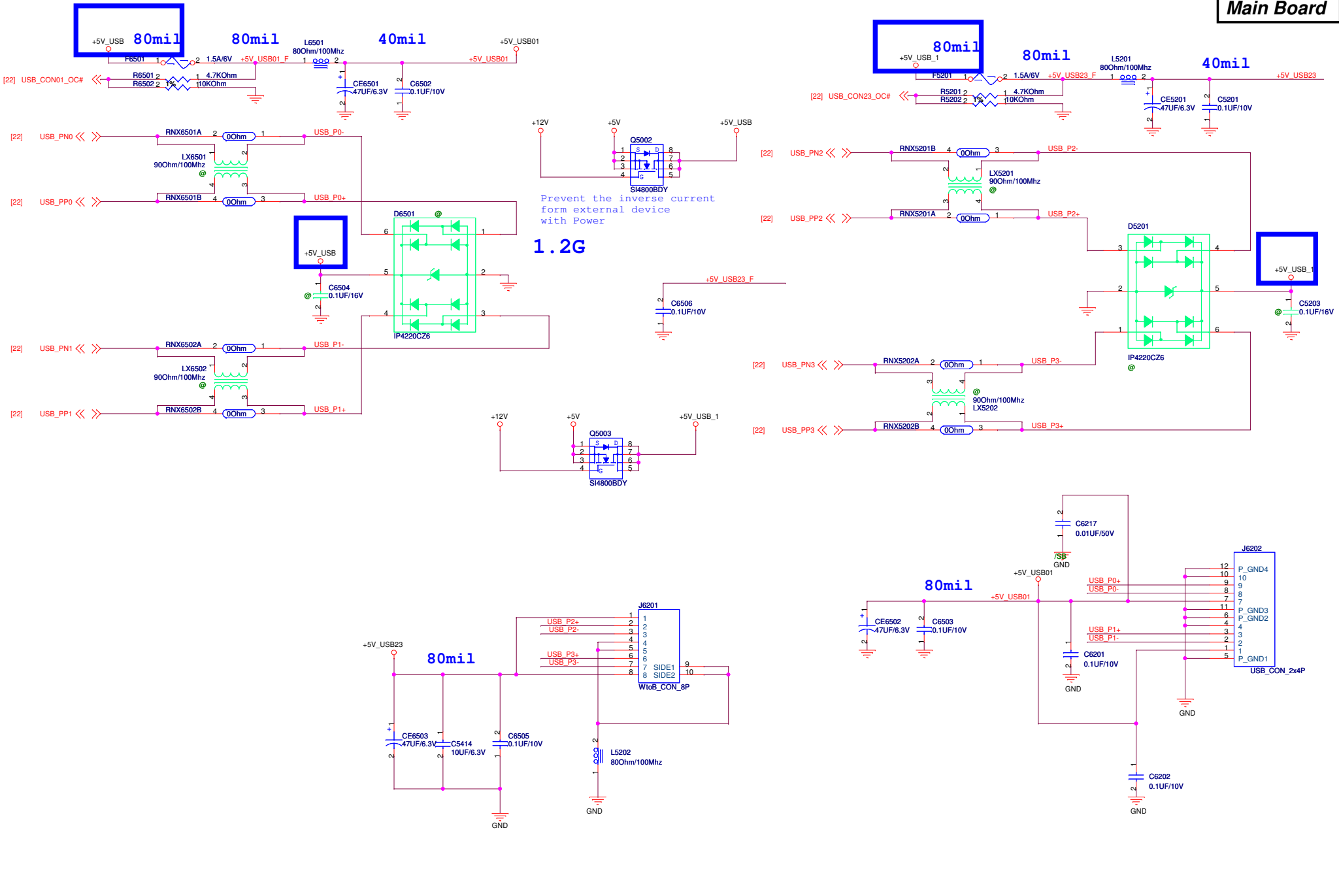
DC FAN Control



ODD

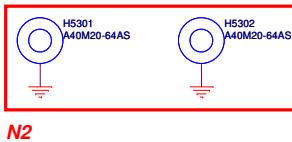
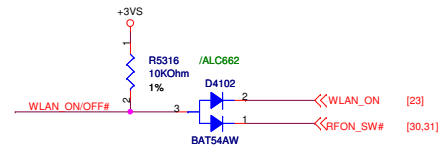
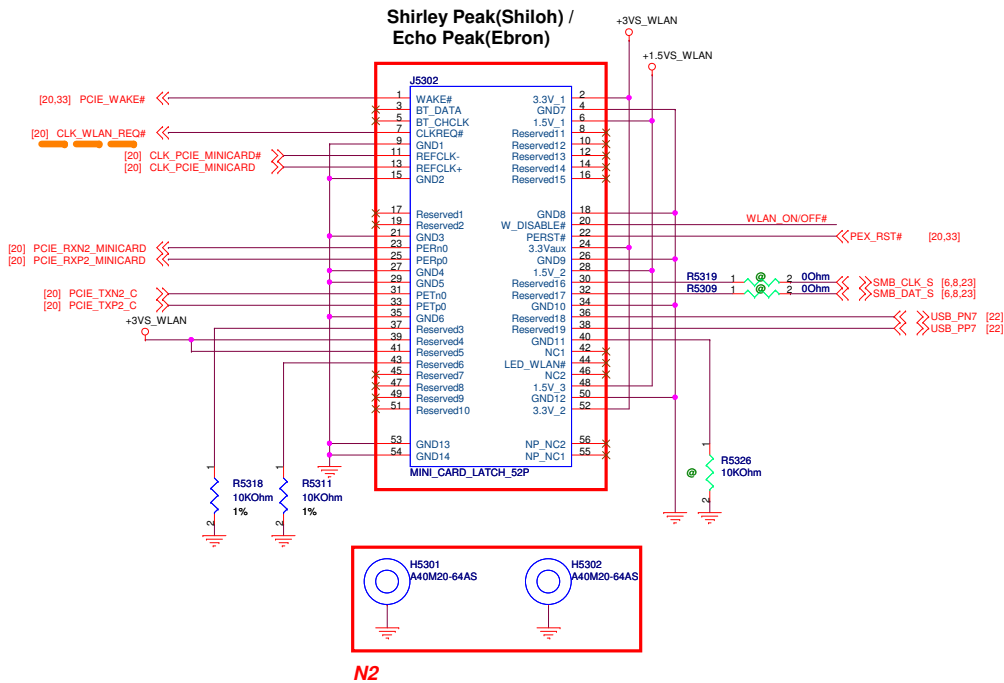
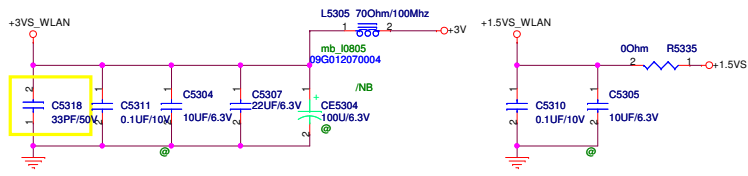


-Variant Name-		
ASUS		Title Sata HDD & Swap Bay
Engineer:		
Size	Project Name	Rev
Custom		1.0
Date: Friday, February 13, 2009	Sheet 51 of 91	



<Variant Name>

ASUS		Title : USB_USB Ports	
ASUSTeK COMPUTER INC. NBI		Engineer: Vincent Chung	
Size Custom	Project Name G71V	Date: Friday, February 13, 2009	Rev 1.0
Sheet 52 of 91			



<Variant Name>

ASUS Title :Minicard & Nut
Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, February 13, 2009 Sheet 53 of 91

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<Variant Name>



Title :

Engineer:

Size A	Project Name	Rev 1.0
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Date: **Friday, February 13, 2009** Sheet **55** of **91**

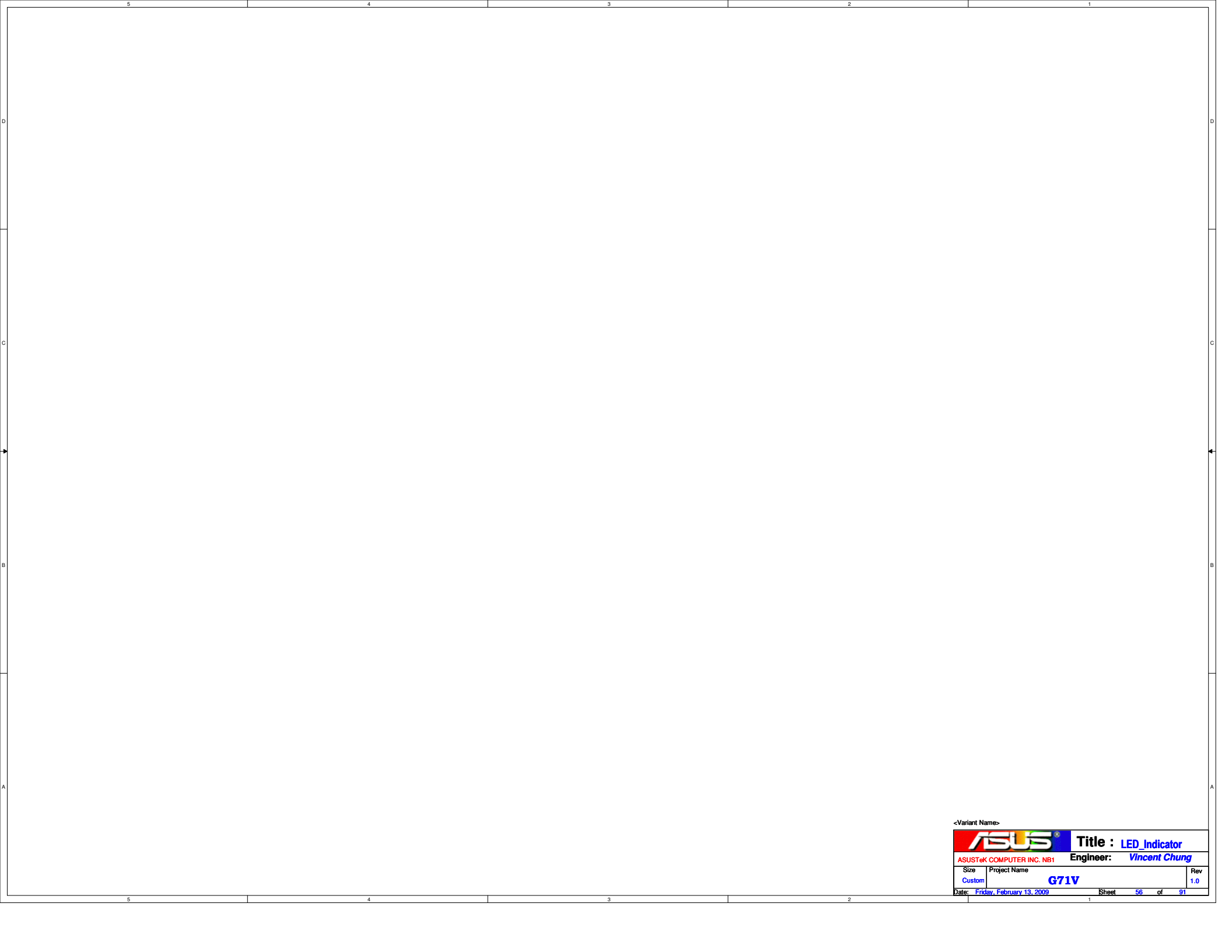
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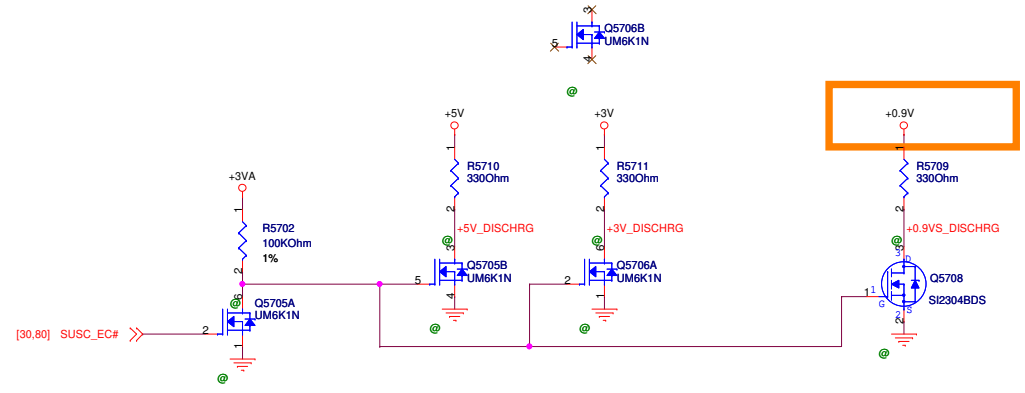
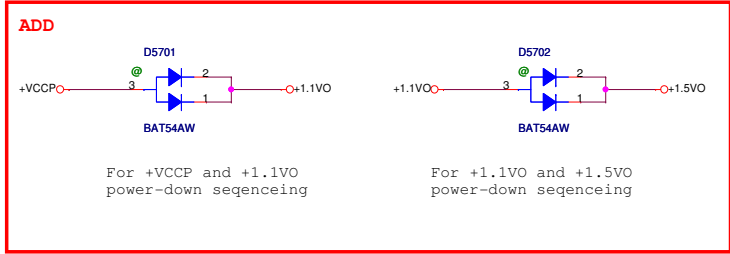
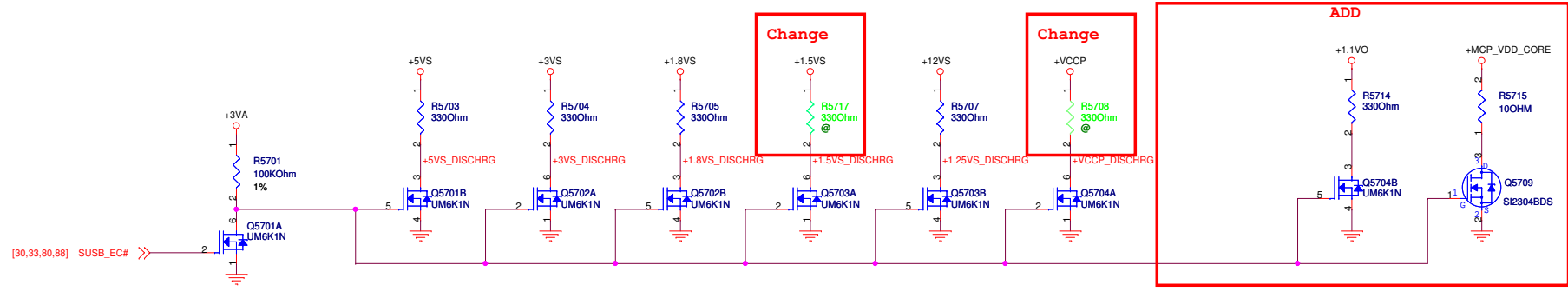
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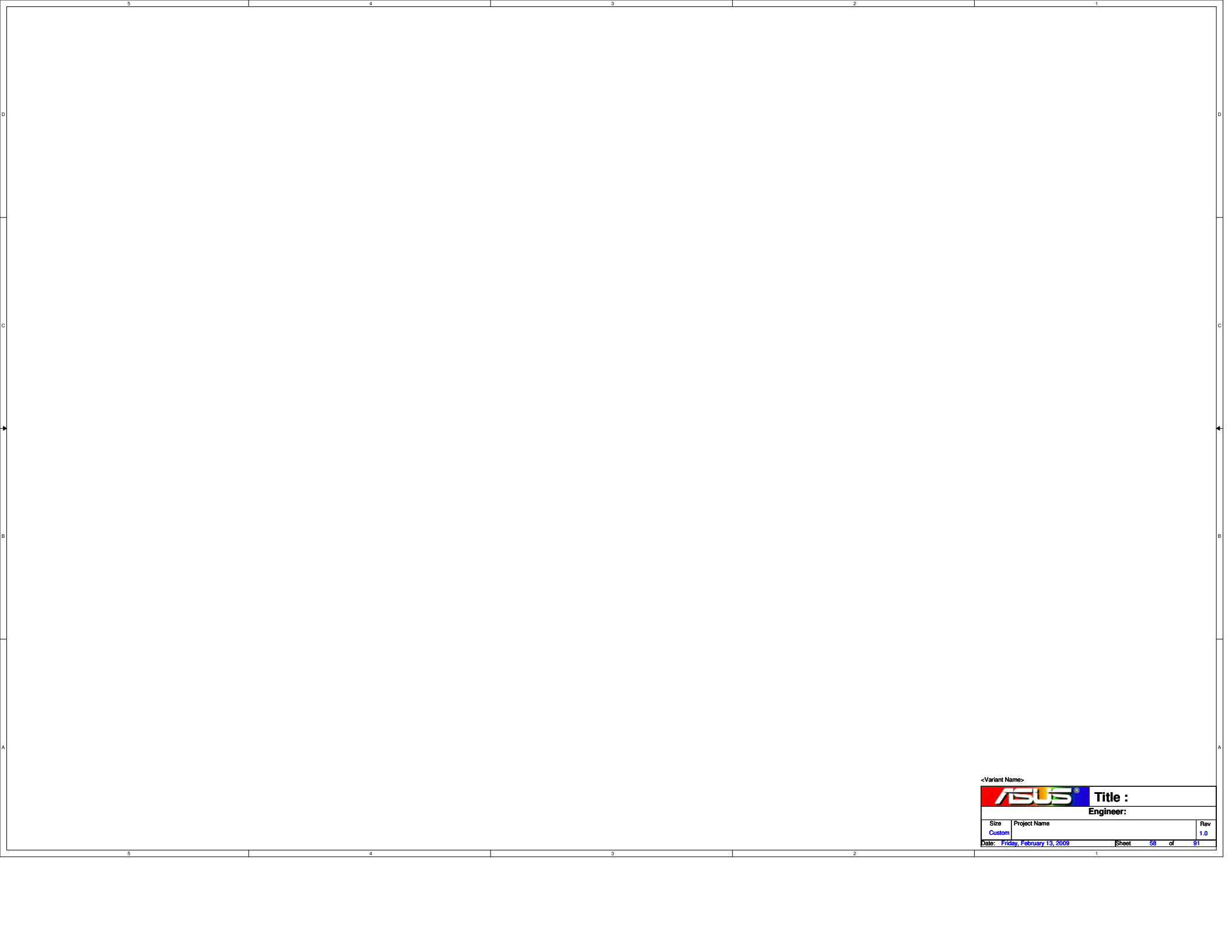
1




<Variant Name>

		Title : LED Indicator	
ASUSTeK COMPUTER INC. NB1		Engineer: Vincent Chung	
Size	Project Name	Rev	
Custom	G71V	1.0	
Date: Friday, February 13, 2009		Sheet	56 of 91





<Variant Name>

		Title :
		Engineer:
Size	Project Name	Rev
Custom		1.0
Date: Friday, February 13, 2009	Sheet 58 of	91

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<Variant Name>



Title :

ASUSTeK COMPUTER INC. NB6 Engineer:

Size A	Project Name	Rev 1.0
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Date: Friday, February 13, 2009 Sheet 59 of 91

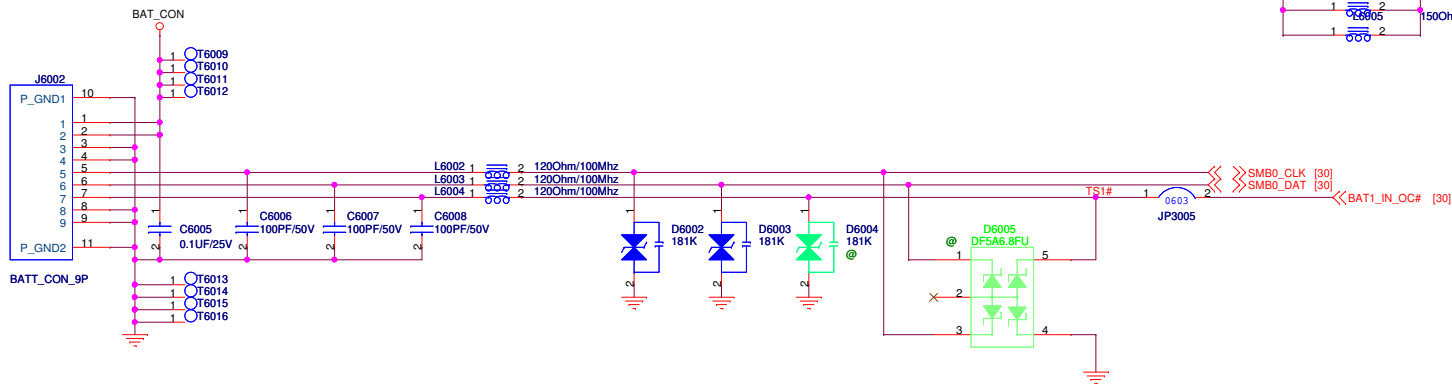
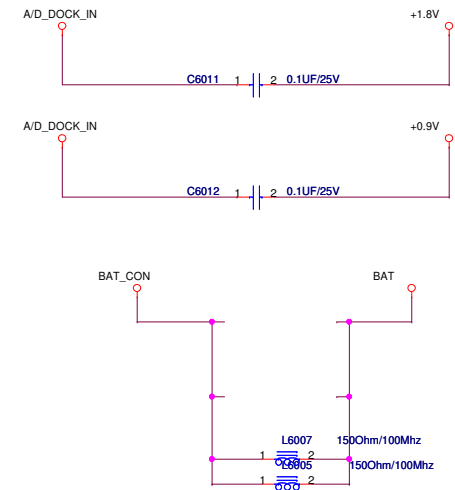
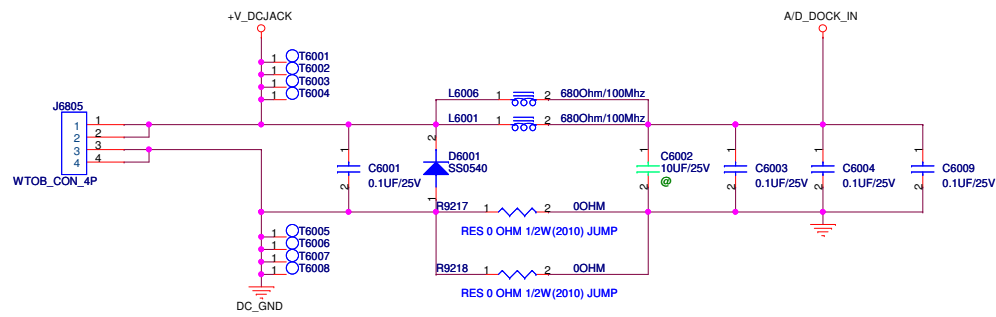
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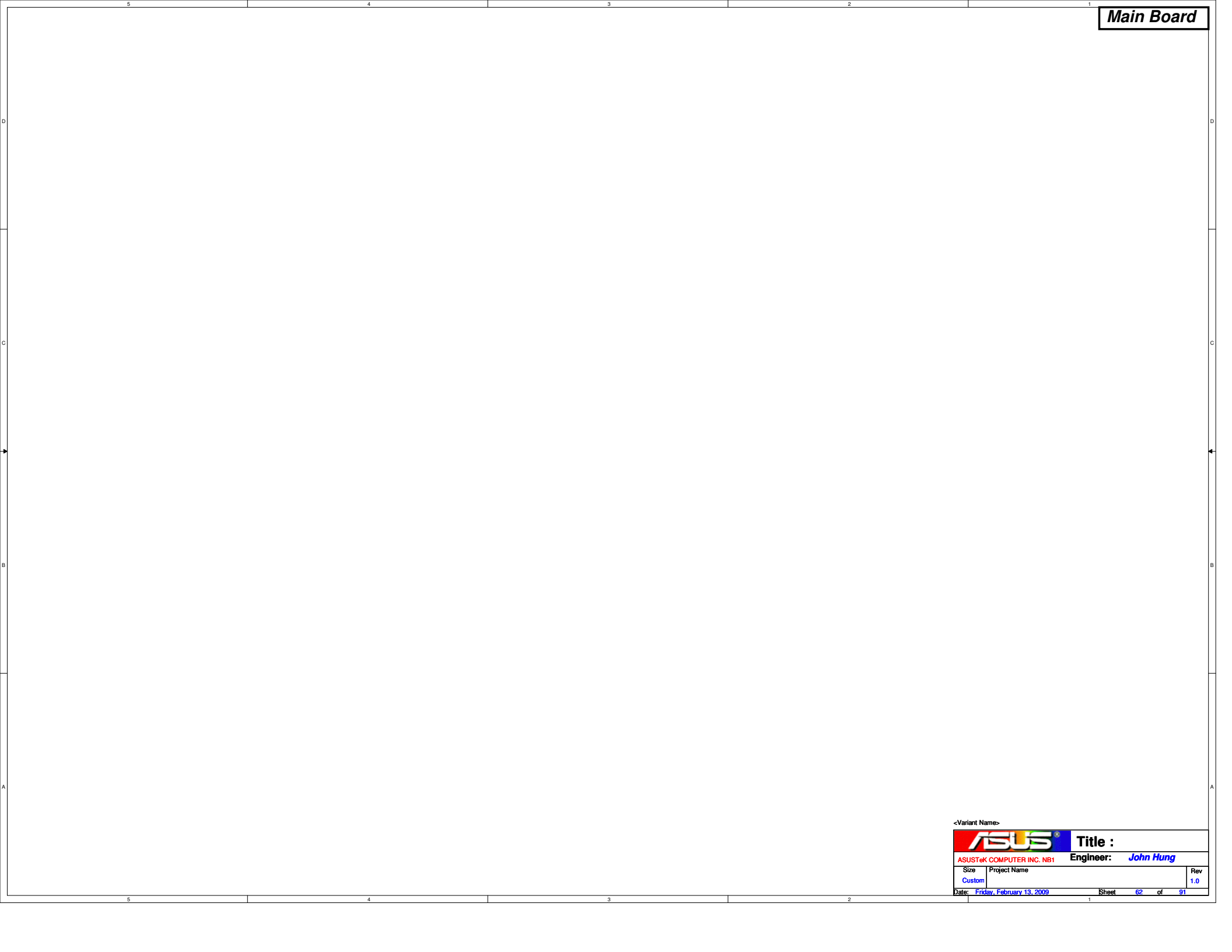
2

1




<Variant Name>

		Title : BT Bluetooth
ASUSTeK COMPUTER INC. NB1		Engineer: Vincent Chung
Size	Project Name	Rev
Custom	G71V	1.0
Date: Friday, February 13, 2009		Sheet 61 of 91



<Variant Name>

		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>John Hung</i>	
Size	Project Name	Rev	
Custom		1.0	
Date: <i>Friday, February 13, 2009</i>		Sheet	62 of 91

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<Variant Name>

		Title : FP_Fingerprint Conn.	
ASUSTeK COMPUTER INC. NB1		Engineer: Vincent Chung	
Size	Project Name		Rev
Custom	G71V		1.0
Date: Friday, February 13, 2009		Sheet	63 of 91

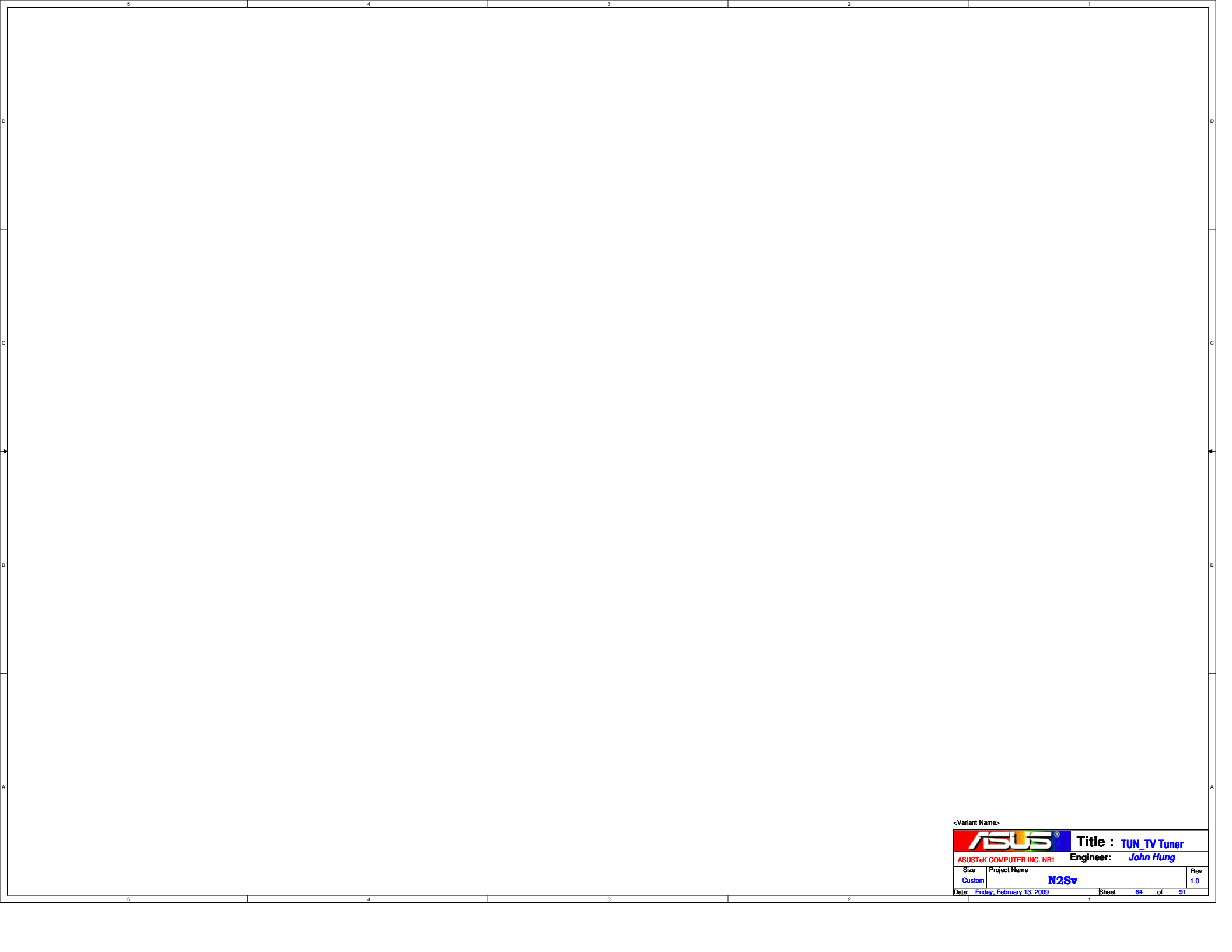
5

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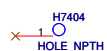
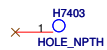
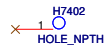
<Variant Name>

		Title : TUN_TV Tuner	
ASUSTeK COMPUTER INC. NB1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	N2Sv	1.0	
Date: Friday, February 13, 2009		Sheet	64 of 91

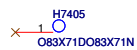
Hole-A



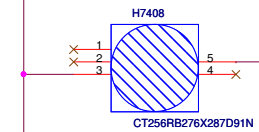
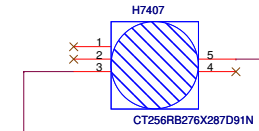
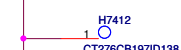
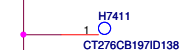
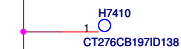
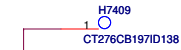
Hole-B



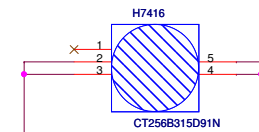
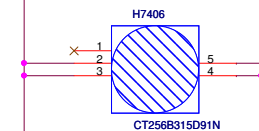
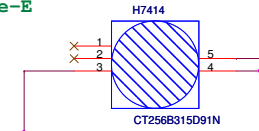
Hole-C



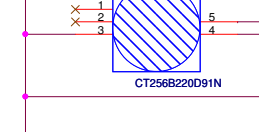
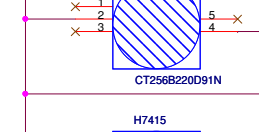
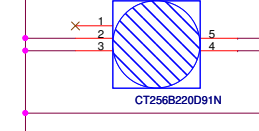
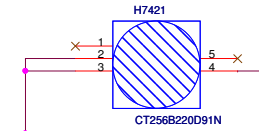
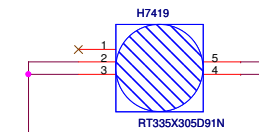
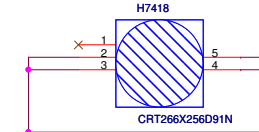
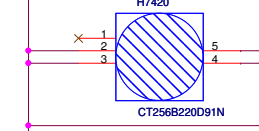
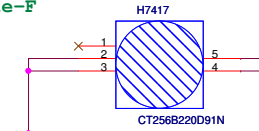
Hole-D



Hole-E



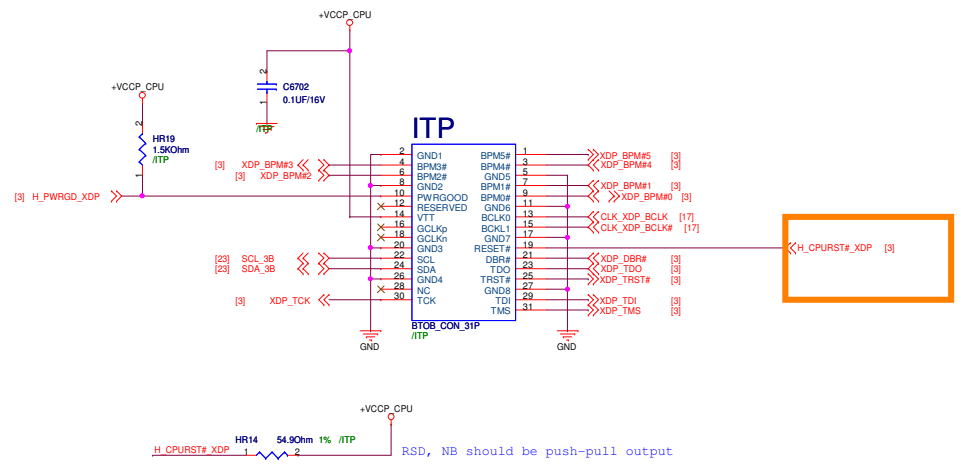
Hole-F



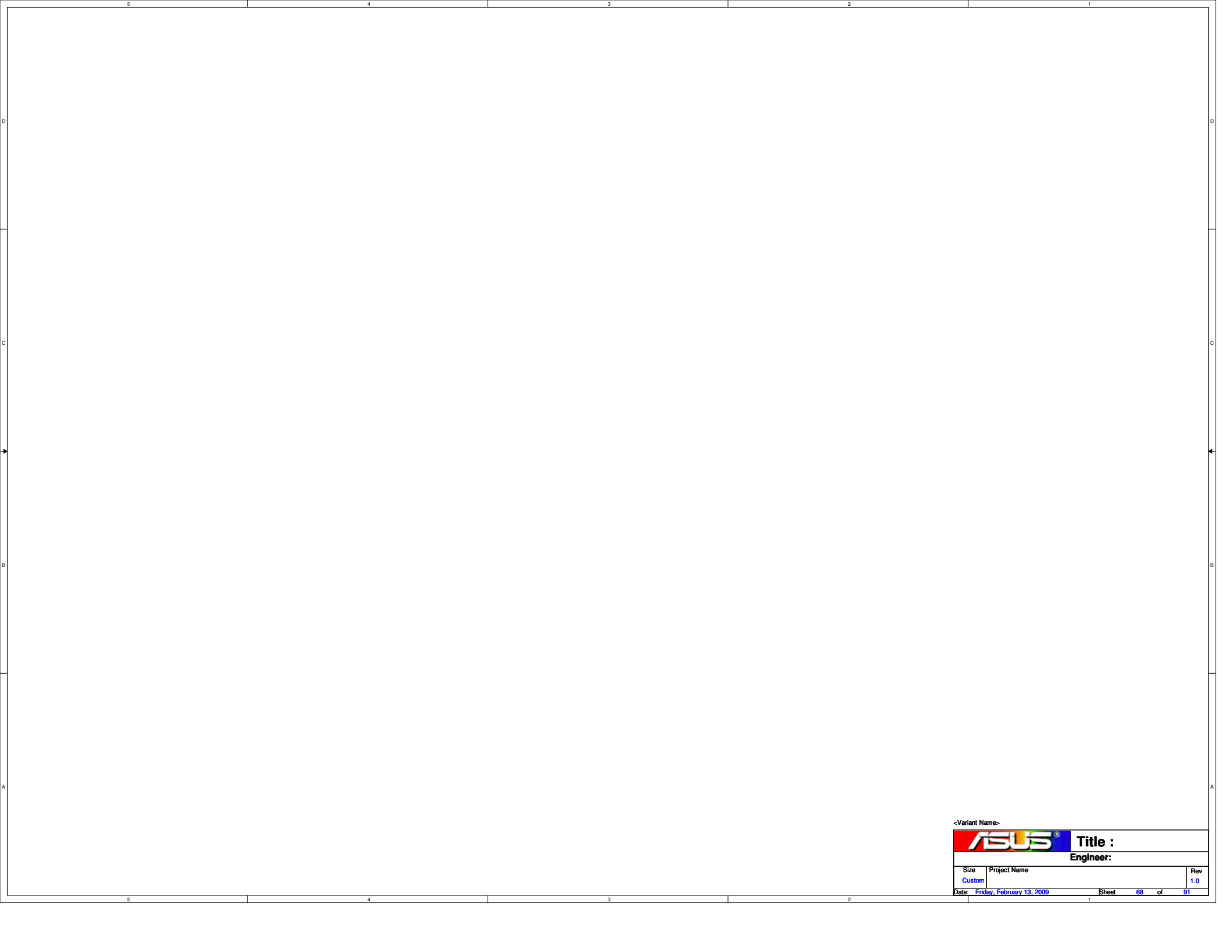
<Variant Name>

		Title :ME_Conn & Screw Holes	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Vincent Chung</i>	
Size Custom	Project Name G71V		Rev 1.0
Date: Friday, February 13, 2009		Sheet	65 of 91


Place Beside CPU




~~IN CPU page~~



<Variant Name>

		Title :
Engineer:		
Size	Project Name	Rev
Custom		1.0
Date: Friday, February 13, 2009	Sheet 68 of	91



		Title :N10M-GE1_PCIE	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name	Rev	
Custom	N10JG	1.0	
Date: Friday, February 13, 2009		Sheet	69 of 91



		Title :N10M-GE1_FB	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
Custom	N10JG		1.0
Date: Friday, February 13, 2009		Sheet	70 of 91

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		Title :N10M-GE1 VRAM	
ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size	Project Name		Rev
Custom	N10JG		1.0
Date: <i>Friday, February 13, 2009</i>		Sheet	71 of 91

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		Title :N10M-GE1_DISPLAY	
ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size	Project Name	Rev	
Custom	N10JG	1.0	
Date: <i>Friday, February 13, 2009</i>		Sheet	72 of 91

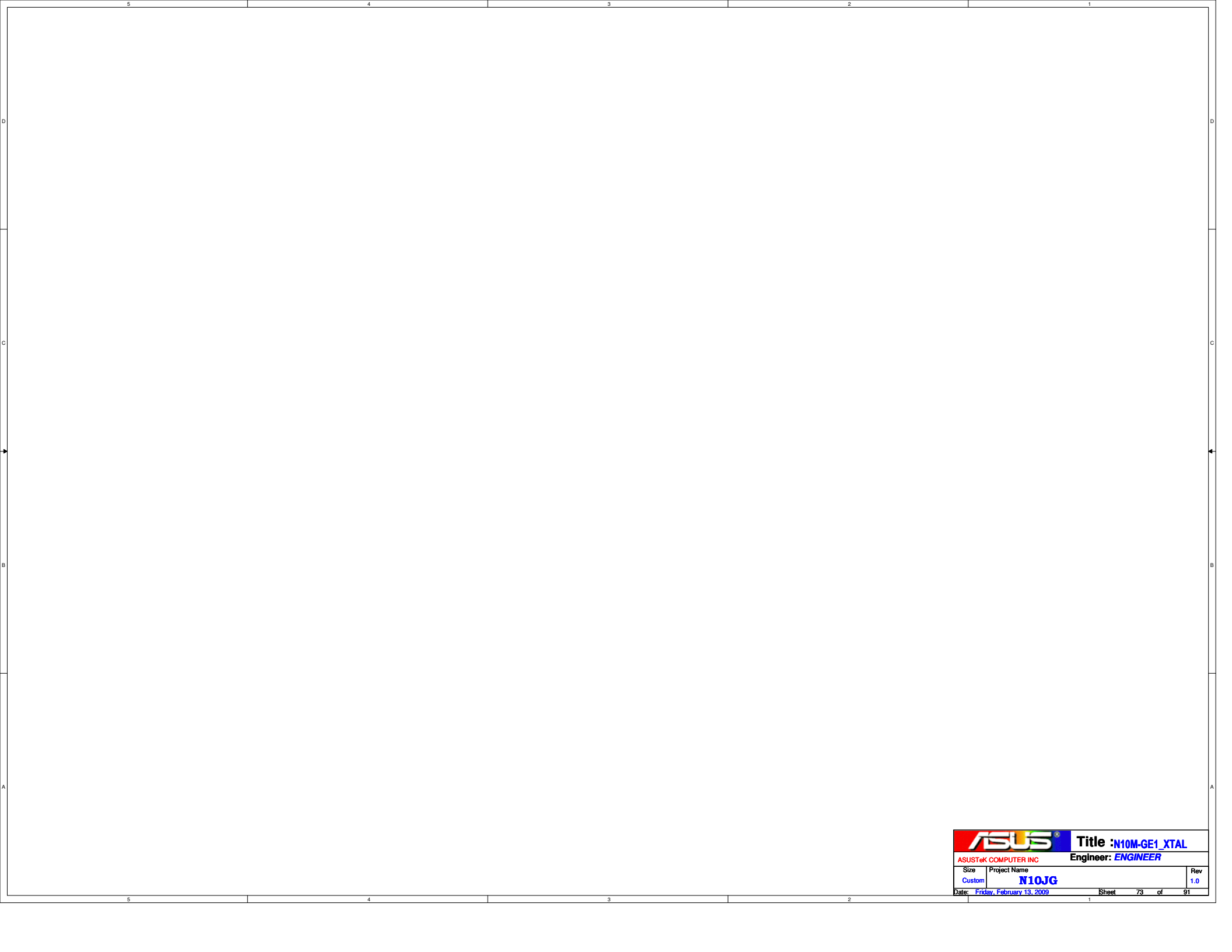
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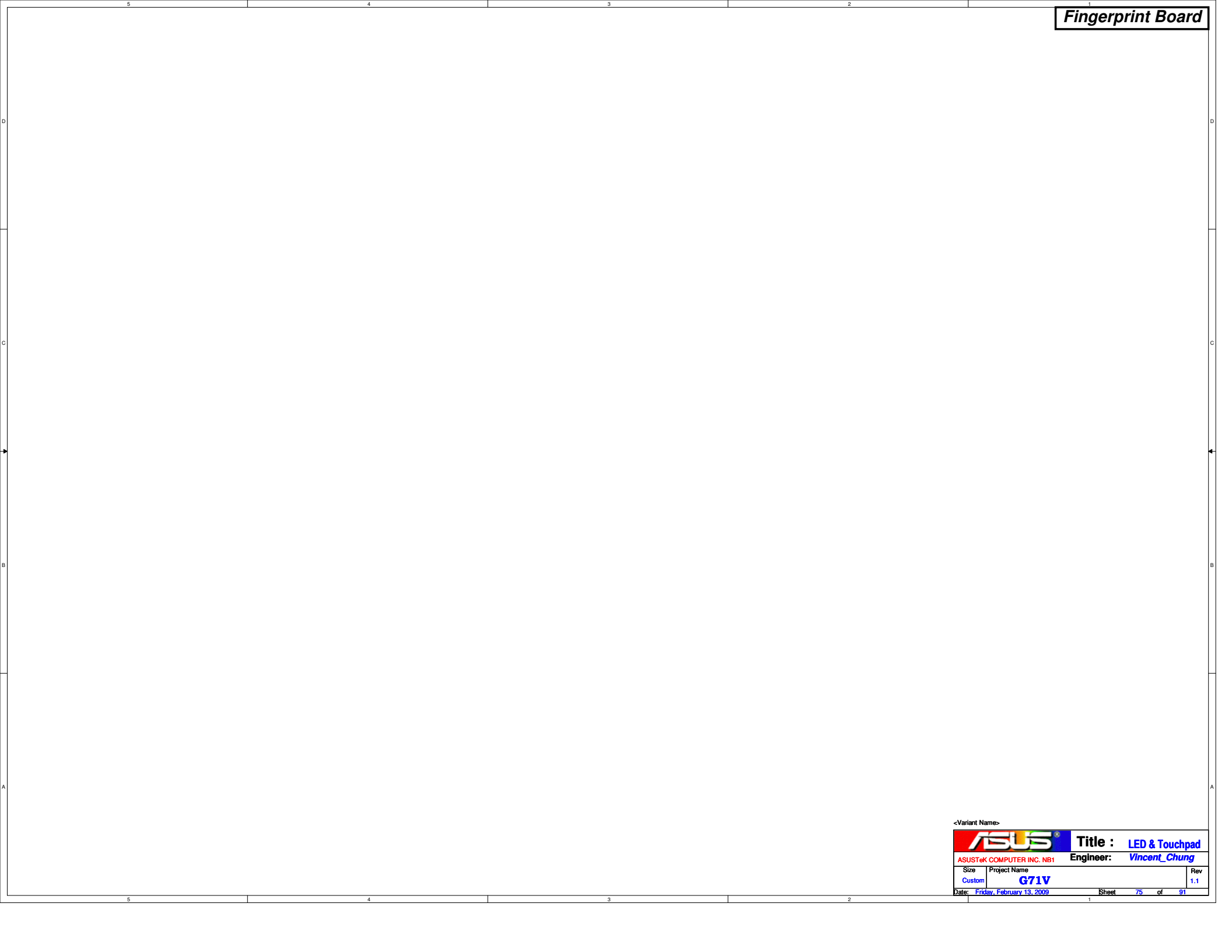
1




		Title :N10M-GE1_XTAL	
ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size	Project Name		Rev
Custom	N10JG		1.0
Date: <i>Friday, February 13, 2009</i>		Sheet	73 of 91



		Title :N10M-GE1_ROM	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size	Project Name		Rev
Custom	N10JG		1.0
Date: Friday, February 13, 2009		Sheet	74 of 91




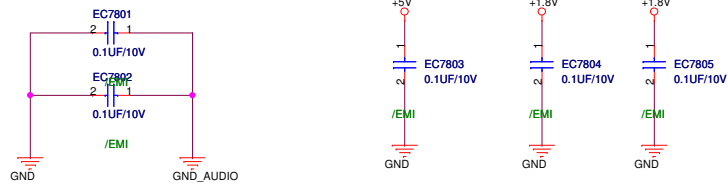
<Variant Name>

		Title : LED & Touchpad
ASUSTeK COMPUTER INC. NB1		Engineer: Vincent Chung
Size	Project Name	Rev
Custom	G71V	1.1
Date: Friday, February 13, 2009		Sheet 75 of 91



<Variant Name>

		Title : Fingerprint & Touchpad
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Wenchi_Shen</i>
Size	Project Name	Rev
Custom	M70Sv	1.1
Date: <i>Friday, February 13, 2009</i>		Sheet 76 of 91



<Variant Name>

		Title :Fingerprint & Touchpad	
ASUSTeK COMPUTER INC. NB1		Engineer: Wenchi_Shen	
Size	Project Name		Rev
Custom	M70Sv		1.1
Date: Friday, February 13, 2009		Sheet	77 of 91

History

1.0G:@

1.1G power modify : \$

1.2G: %

1.1G EE modify :

20080520 1.2G

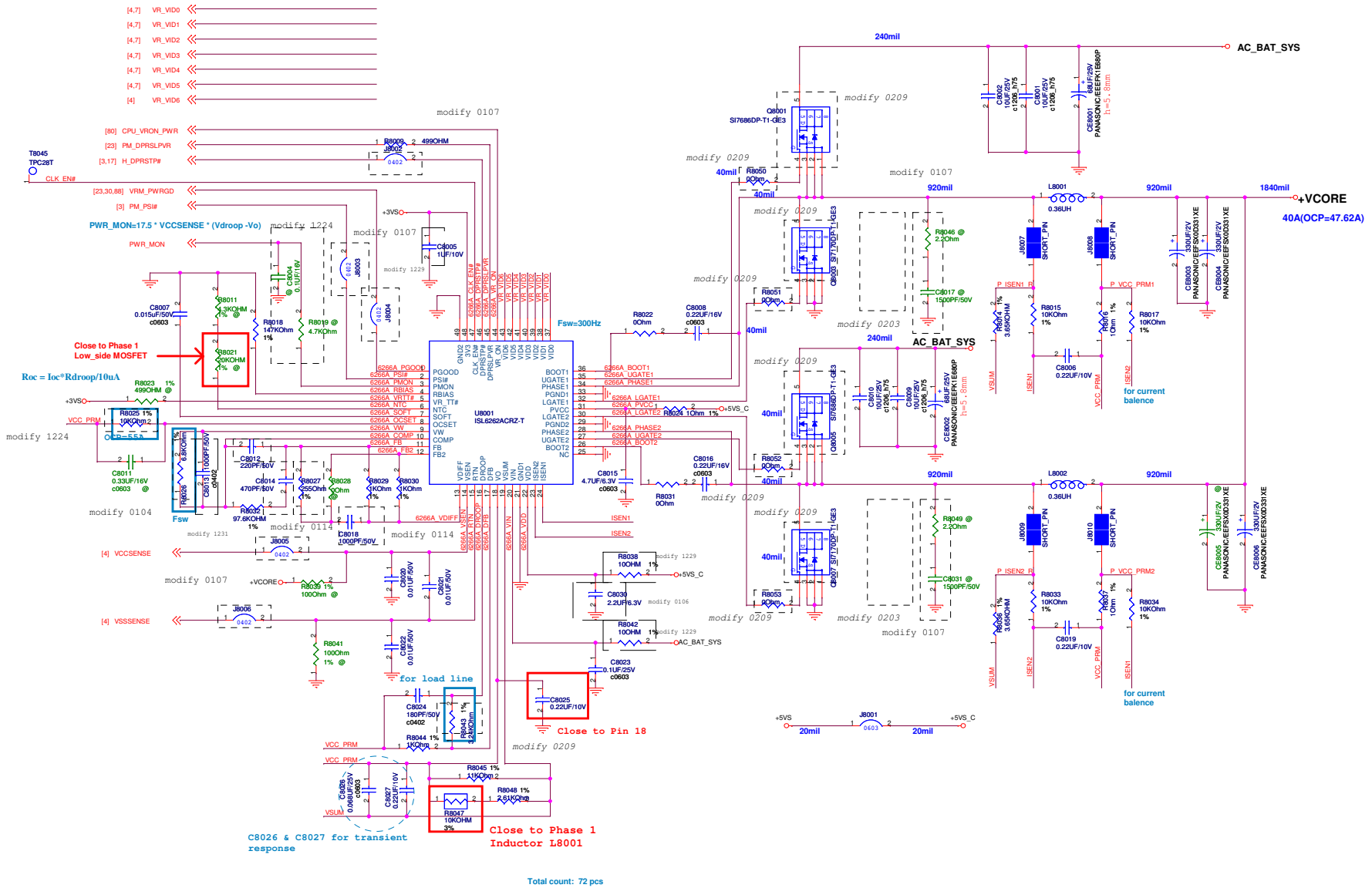
- Page 52 1. ADD USB+5V gate Q5002
- Page 56 2. ADD R5626,R5609
- Page 4 3. DEL R0412
- Page 54 4. ADD C5402,C5403 5p for SMBus in GPIO controller ; GPRN10 change to 10K ohm
- Page 84 5. Controlle +5V with SUSC#_PWR
- Page 82 6. Change +VCCP to 1.2V default for CPU O.C. ability improve

20080701 2.0G

- Page 56 1. TP-LED v.s. TP-disable LED reverse
- Page 45 2. Inverter CN pin 19 reserve 0 phm to GND ,never stuff for single-lamp inverter
- Page 46 3. Battery in P/H change to +3VA
- Page 80 4. CPU load-line modify to 2.1 mini-ohm (R8036 由 10.5K改成 9.31K 1%)

<Variant Name>

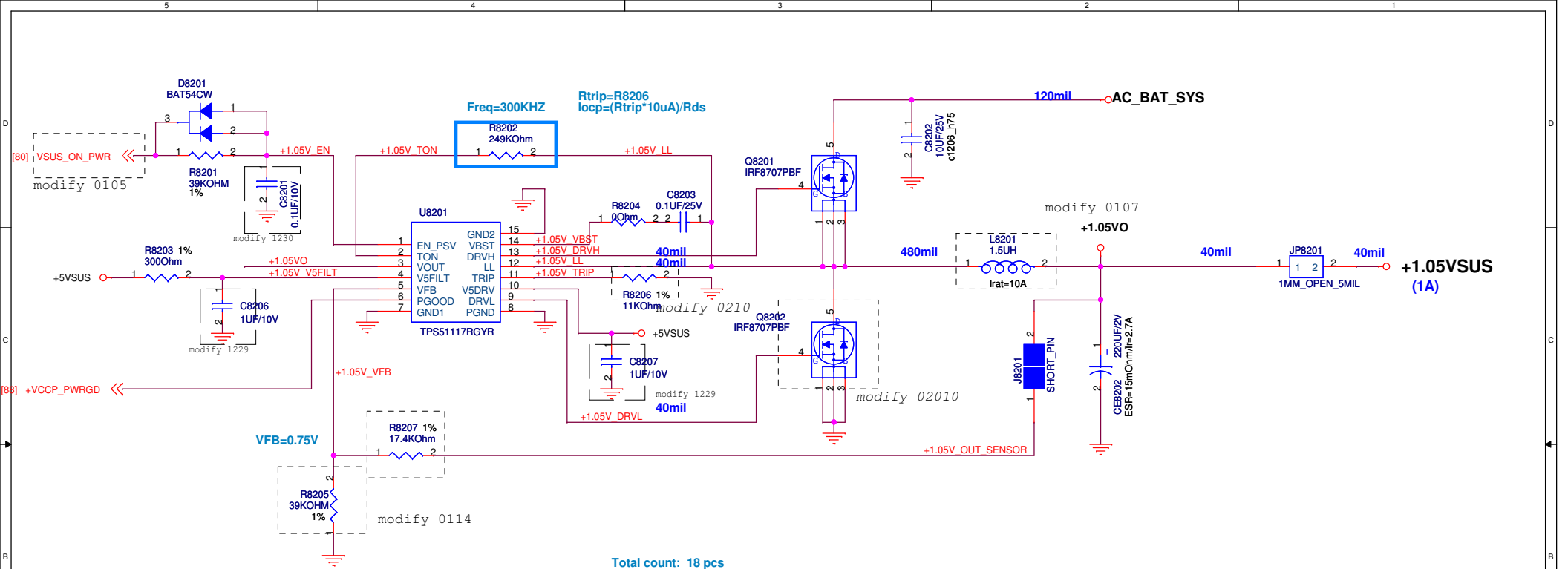
		Title : History	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Friday, February 13, 2009	Sheet	78	of 91



Total count: 72 pcs

HS MOS Second source IRF8714
 LS MOS Second source IRF8736

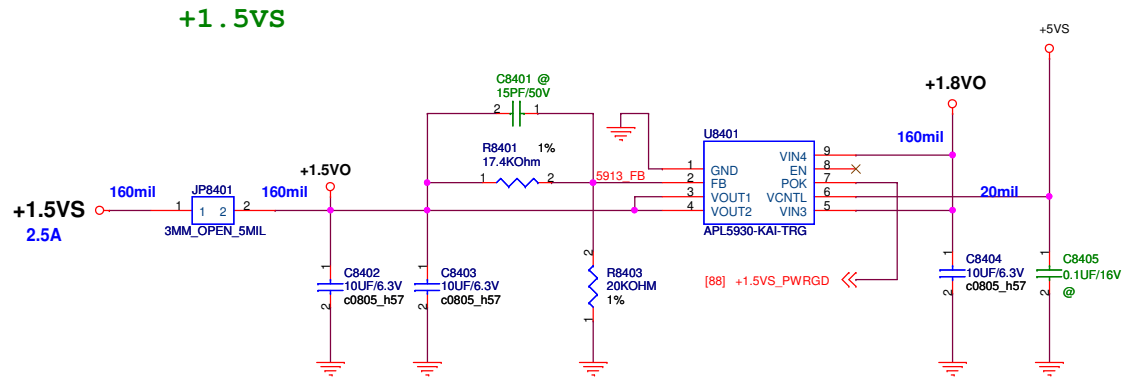
ASUS		Title : +Vcore	
ASUSTek COMPUTER INC. NBI		Engineer: Eason	
Size	Project Name	Rev	
Custom	K501	1.0	
Date: Friday, February 13, 2009	Sheet	79	of 81



Total count: 18 pcs

<Variant Name>

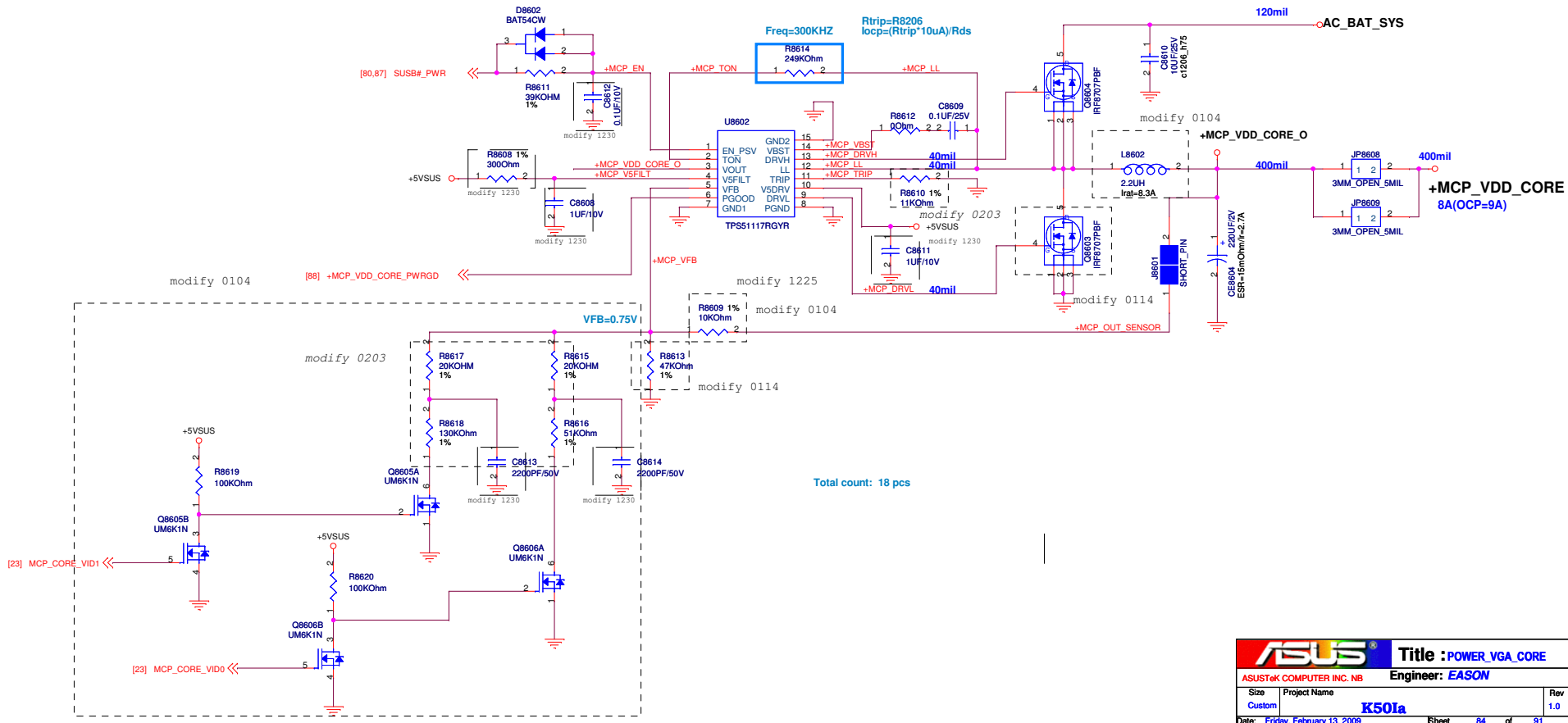
		Title : POWER_I/O_VCCP	
ASUSTeK COMPUTER INC. NB		Engineer: Eason	
Size Custom	Project Name K50I	Rev 1.0	
Date: Friday, February 13, 2009		Sheet 81 of 91	

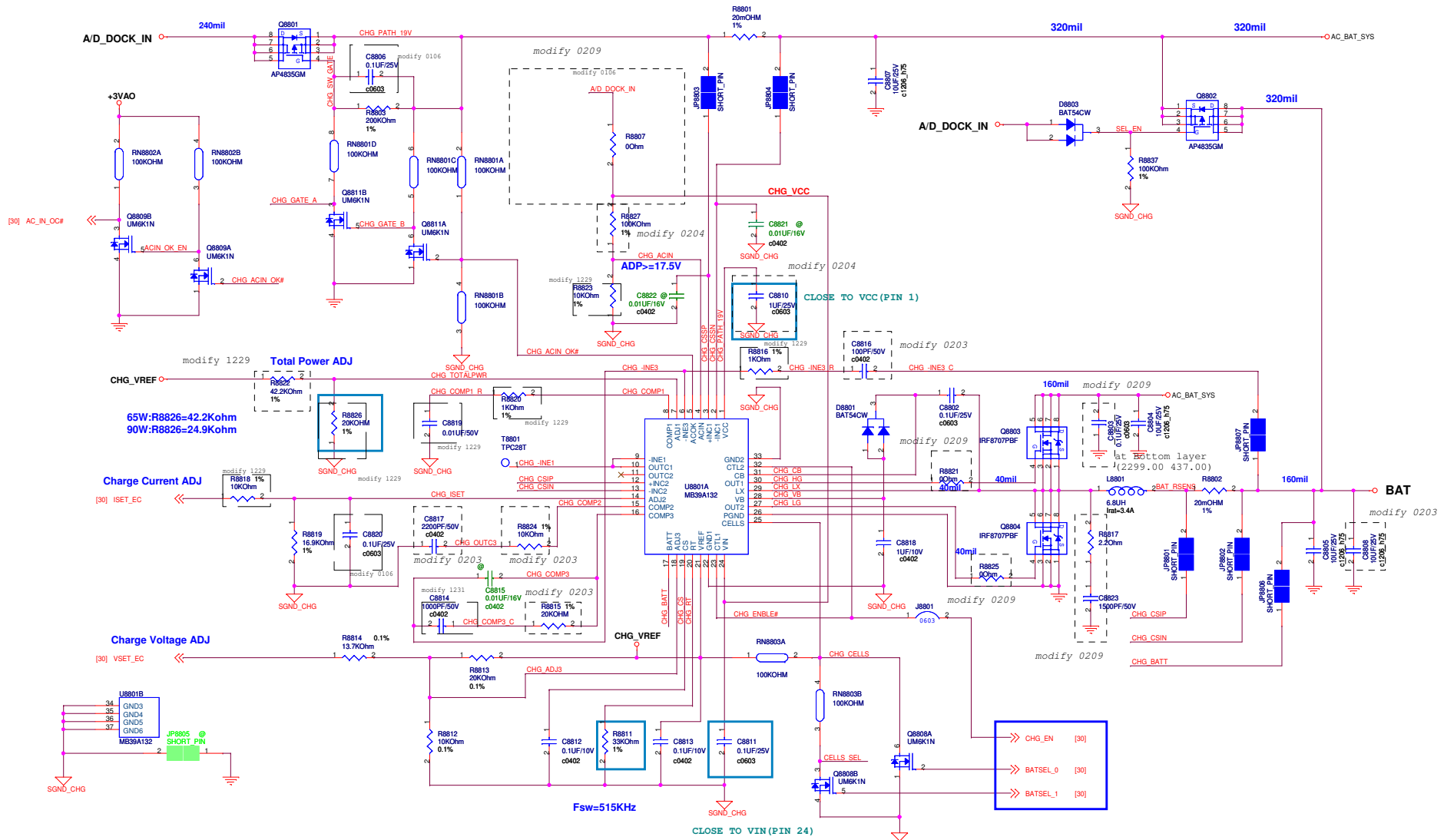


Total count: 6 pcs

<Variant Name>

ASUS		Title : INS29491694
ASUSTeK COMPUTER INC. NB		Engineer: Eason
Size B	Project Name K50I	Rev 1.0
Date: Friday, February 13, 2009		Sheet 83 of 91





TOTAL COUNT:56 PCS

Battery Cells		
BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
H	L	2 CELLS
L	H	3 CELLS
L	L	4 CELLS

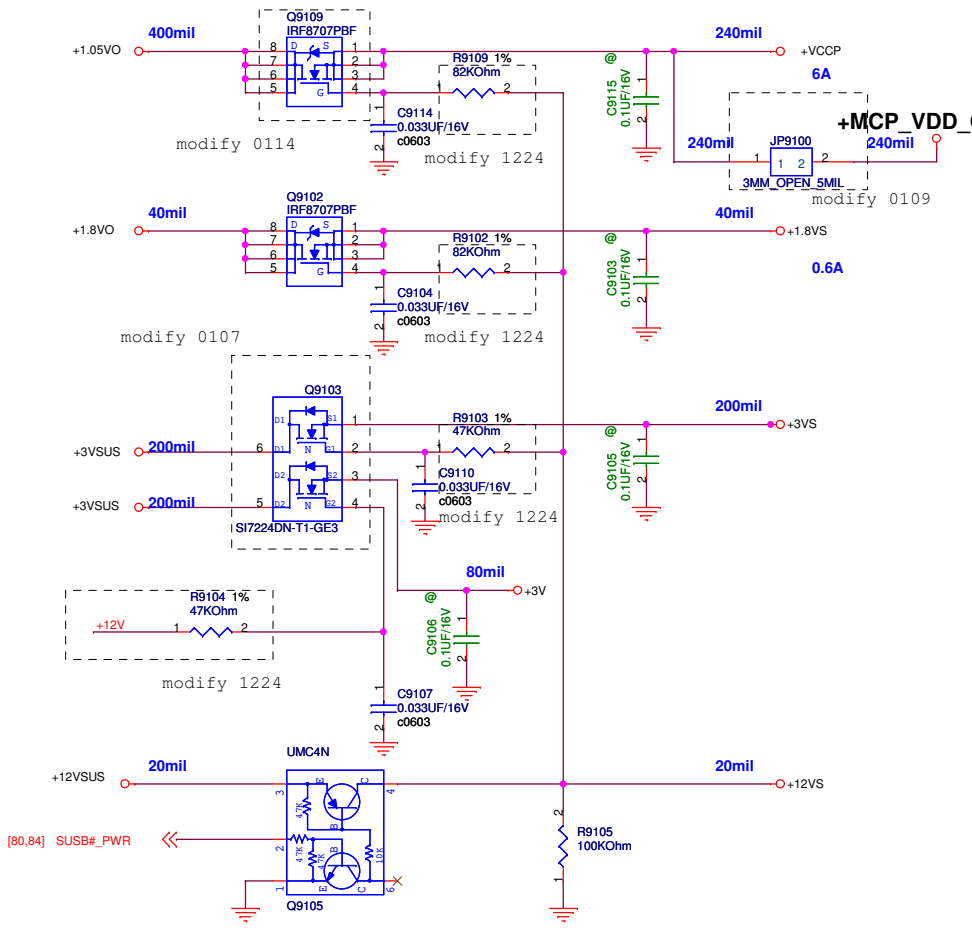
Charger IC and EC Code correlation sheet :
 Charger MAX8725 => EC CODE : 200
 Charger MAX17015 => EC CODE : 201
 Charger MB39A132 => EC CODE : 202

BATTERY IN DETECT

<Variant Name>

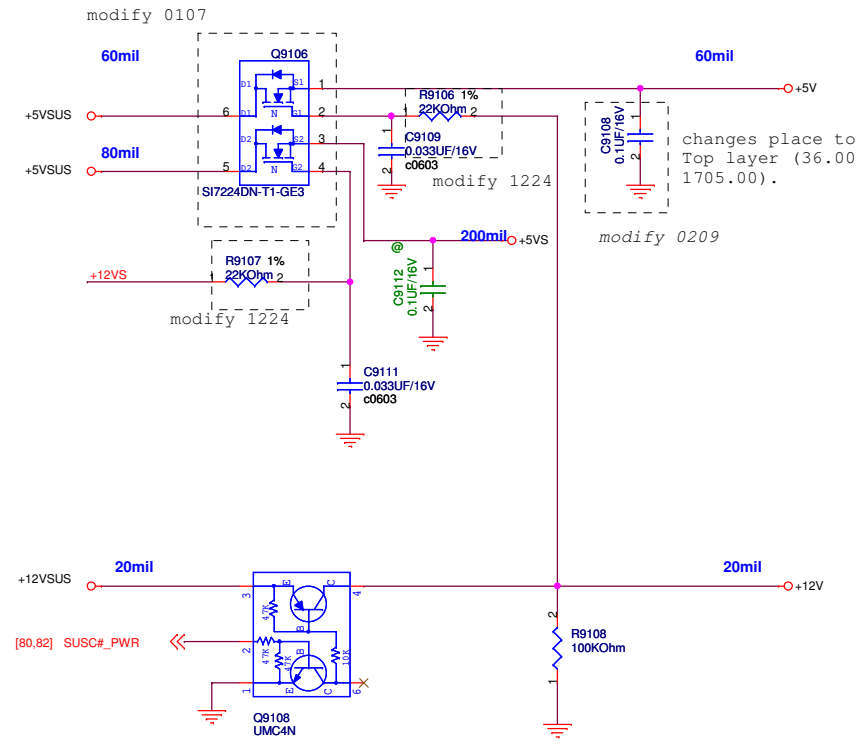
		Title :POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: Eason	
Size	Project Name		Rev
Custom	K50I		1.0
Date: Friday, February 13, 2009		Sheet	86 of 91

SUSB#_PWR POWER



Total count: 19 pcs

SUSC#_PWR POWER

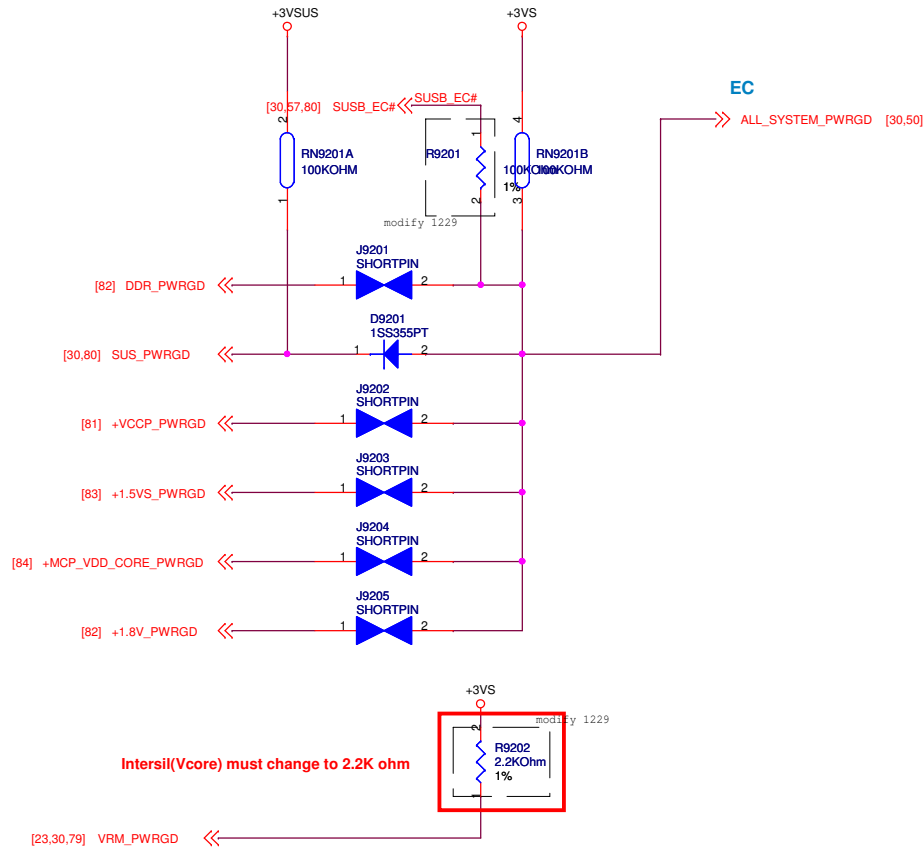


changes place to Top layer (36.00 1705.00).

<Variant Name>

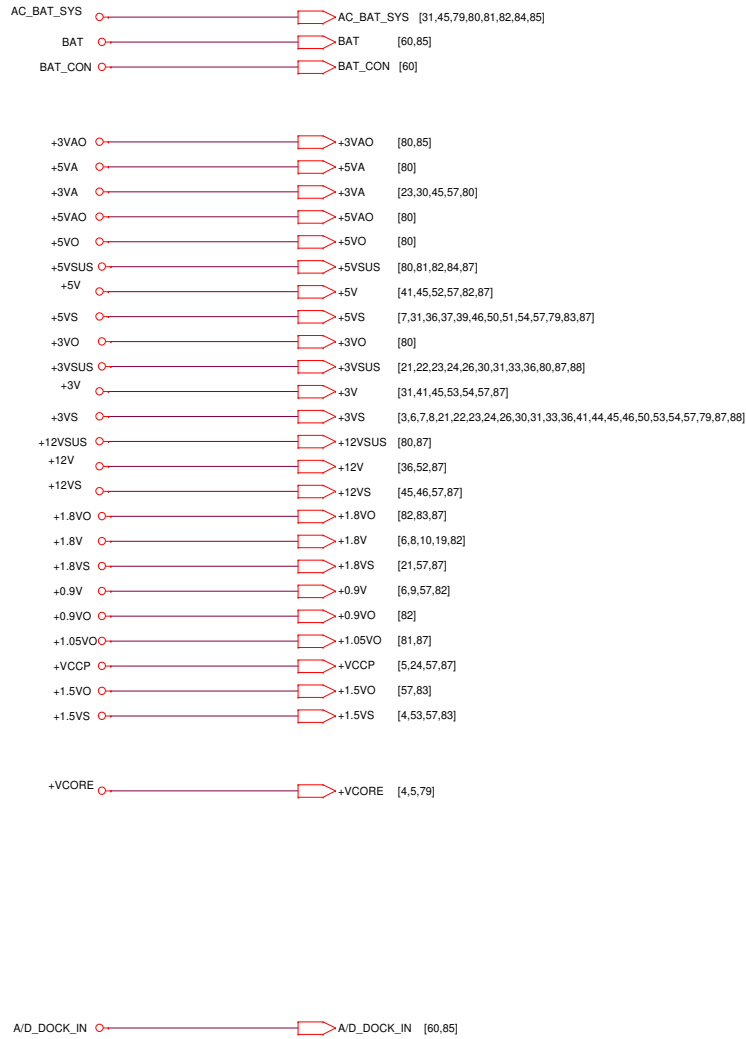
ASUS		Title : POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: Eason	
Size B	Project Name K50I	Date: Friday, February 13, 2009	Rev 1.0
		Sheet 87 of 91	

POWER GOOD DETECTOR



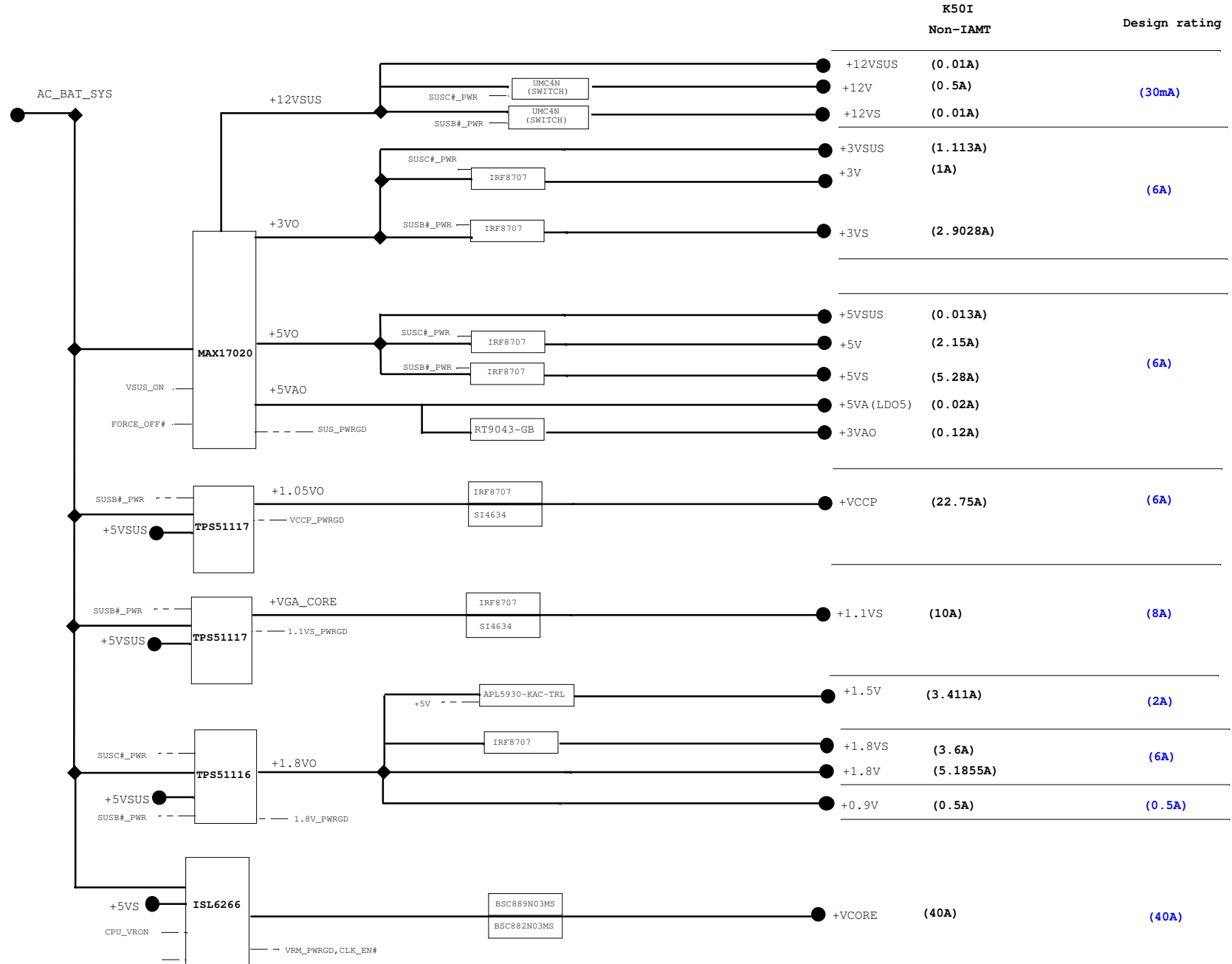
Total count: 8 pcs

<Variant Name>		ASUS		Title : POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Eason			
Size B	Project Name K50I			Rev 1.0	
Date: Friday, February 13, 2009		Sheet 88 of 91			



<Variant Name>

		Title : POWER_SIGNAL	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Eason</i>	
Size Custom	Project Name K50I		Rev 1.0
Date: Friday, February 13, 2009	Sheet	89	of 91



K50I		Design rating
Non-IAMT		
+12VSUS	(0.01A)	
+12V	(0.5A)	(30mA)
+12VS	(0.01A)	
+3VSUS	(1.113A)	
+3V	(1A)	(6A)
+3VS	(2.9028A)	
+5VSUS	(0.013A)	
+5V	(2.15A)	(6A)
+5VS	(5.28A)	
+5VA (LDO5)	(0.02A)	
+3VAO	(0.12A)	
+VCCP	(22.75A)	(6A)
+1.1VS	(10A)	(8A)
+1.5V	(3.411A)	(2A)
+1.8VS	(3.6A)	(6A)
+1.8V	(5.1855A)	
+0.9V	(0.5A)	(0.5A)
+VCORE	(40A)	(40A)

VR_VID0-VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLEWR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON

